For fast analog signals build a 50-MHz data acquisition system

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In data-acquisition tasks, higher analog-to-digital conversion rates are an absolute necessity for accurately processing analog signals. Fortunately, building such a data-acquisition system from off the shelf components is easier, thanks to the availability of microprocessors and signal-processing chips with the requisite speed, capacity, and accuracy requirements.

A flash a-d converter with ECL memory and logic circuitry is employed in a data-acquisition system that converts up to 50 million samples per second. Thus, it captures transients with frequency components as high as 25 MHz. Its memory-mapped interface, with 4096 bytes of on-board memory, is compatible with most microprocessor layouts so it will find wide use in tasks involving transient waveform analysis, video signal conversion, and general purpose high-speed data handlers.

An 8-bit flash converter and 4 Kbytes of ECL memory form an instrument-grade data-acquisition system suitable for transient capture.

The basic parts of the system (Fig. 1) include the data conversion and memory block; variable gain input amplifier; system clock and address counter; system interface and control circuitry; and the stages for supplying power to the system.

The a-d converter is the most important element since the characteristics of the data sampling device, the a-d converter, ultimately set the capabilities of a data acquisition system. Flash converters are ideal for this application, operating well into the megahertz region.

The flash converter achieves its high speed by directly transforming an input analog signal to digital format by means of a totem-pole type arrangement of 255 separate analog comparators (for an 8-bit converter) biased by a common resistive divider setting their threshold (reference) points. A reference voltage is placed across the network to supply a unique firing voltage for each comparator. This reference voltage establishes the dynamic range (maximum input voltage) that can be encoded by the converter circuitry. As input voltage increases, the comparators turn on in succession. Their collective output is then converted to an 8-bit digital output by means of a 255-to-8 line encoder, and then latched.

The converter selected for this system is TRW's TDC1025, an 8-bit device working at conversion rates exceeding 50 MHz. The least discernible, or quantum, signal for this converter over a 2-V input voltage range is equal to the input voltage range (2 V) divided by the number of discrete intervals (2^8 - 1), or 7.8 mV. This value is also the quantization error and represents the practical lower limit of ripple voltage riding on the input signal that can be encoded for the given dynamic range. However, the actual dynamic range can be set via the converter's RT and RB pins.

The voltage applied to the RB pin sets the maximum voltage the converter recognizes; on the RT pin, this determines minimum voltage. In this particular case, the RB pin is connected to a -2 V source and the RT pin is grounded.

The signal-to-noise (s/n) ratio as measured at the output of this converter is equal to that of any other similar 8-bit converter, approximately (6n + 2) dB where n is the number of bits of resolution.

Ideally, this results in a signal-to-noise ratio of 50 dB. In practice, the s/n ratio is primarily a function of the frequency and band width of the input signal. For the TDC1025 converter, the s/n ratio is 44 dB for an input frequency of 1.25 MHz and bandwidth of 20 MHz; 42 db at 5.34 MHz; and 38 dB from 10 to 12 MHz. These s/n values correspond to 7.02, 6.68, and 6.02 effective bits of resolution, respectively.

To preserve the dynamic range and bandwidth of

the system, a wideband amplifier such as Harris' HA-2539 should be used in the variable-gain input amplifier stage. It has a slew rate of 600 V/μs and a gain-bandwidth product of 600 MHz. Such amplifiers can be a source of instability if not used properly. The HA-2539, in particular, should be operated with a minimum closed-loop gain of 10 to ensure stability.

In this system, the HA-2539 drives a medium-gain transistor, the 2N2907 which is configured as an emitter follower, to establish the XV_{in} signal. The emitter lead is suitably clamped with a 1N4148 diode.

A general-purpose LM148 op amp in a unity-gain feedback loop with a second 2N2907, develops the dc voltage, RB, necessary to set the dynamic range of the a-to-d converter.

Processed samples from each output of the a-d converter drive a bank of random access memories. Eight Hitachi HM-2142 devices are used, each storing 4K of data, arraged as 4096-by-1. The conversion block requires only the TDC1025 flash converter and eight identical memories connected in rudimentary fashion. More specifically, the XV_{in} signal derived from the aformentioned input amplifier circuit drives each input line of the TDC1025 adc through a corresponding 10-ohm resistor. The RB signal, also derived from the input amplifier, and the convert and $\overline{\text{convert}}$ commands required to initiate a data conversion, are applied to the appropriate lines of the a-d converter.

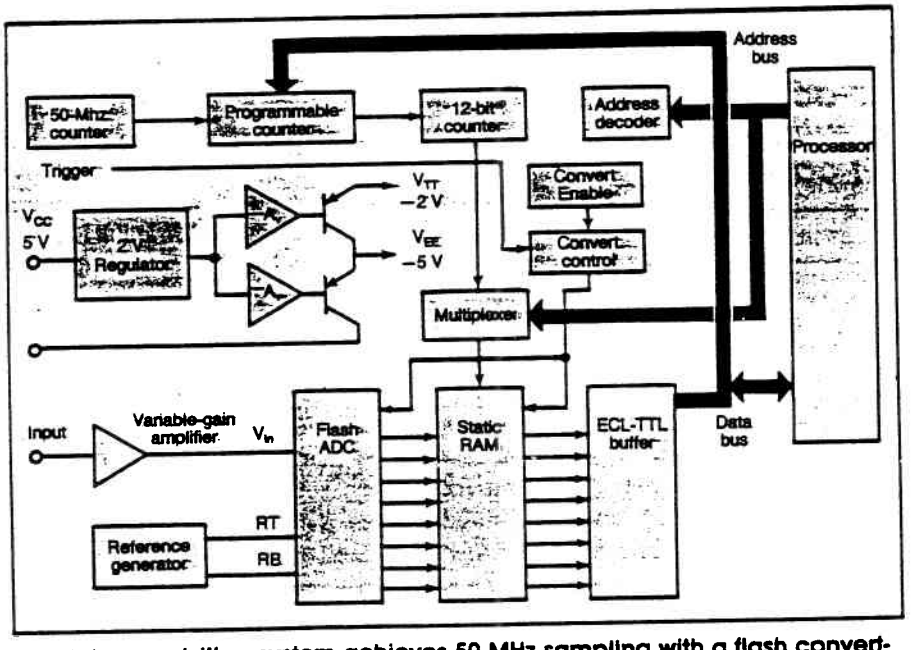
The HM-2142 memories are cascaded (control lines are required in parallel), as are the remaining signal and control lines (such as XR/XW) for those memories. Driving the 12 control ports of the most significant memory are the A_0I at $A_{11}I$ lines of the system clock and control circuit. The outputs of the memories, XD_0A-XD_7A, drive the 10125 MECL-to-TTL translators in the interface section. Read or write operations are performed within 10 ns.; about twice as fast as conventional MOS or CMOS memory chips.

INTERFACE CIRCUITRY PUTS IT TOGETHER

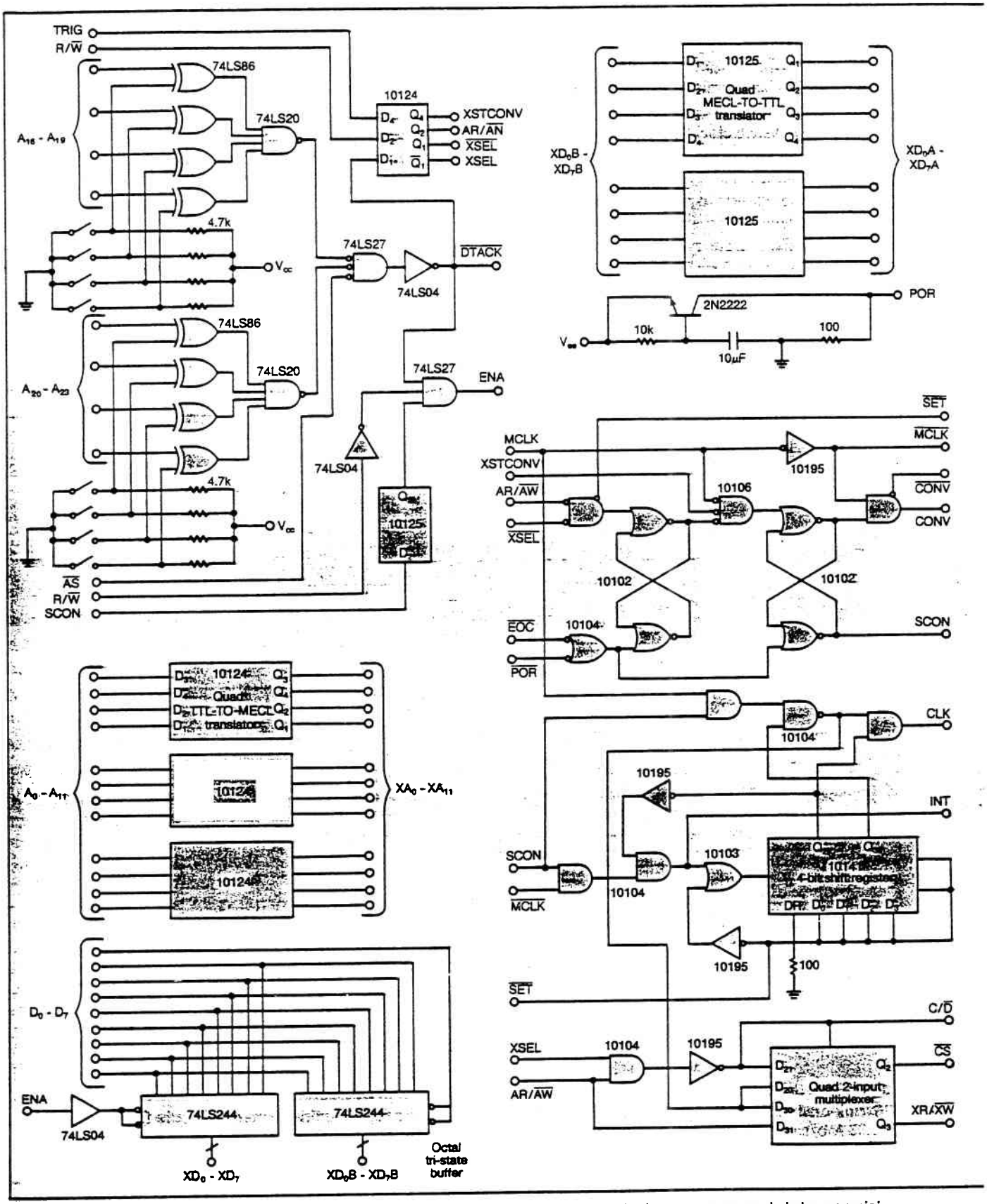
The interface and control circuitry (Fig. 2) merges the ECL logic circuitry with a TTL-compatible bus. This block orchestrates the flow of data to and from the processor and data converter.

Owing to the pipeline arrangement of the converter, data appearing at the output bus lines has a two sample delay. In operation, input samples are applied to the a-d converter during one clock (CONV) cycle, encoded in the next, and placed on the output bus on the third cycle. The basic task of the interface and control circuitry, therefore, is to coordinate system timing.

In general operation, bidirectional lines D_0-D_7 serve to shuttle data and commands between the central processor and the data-acquisition system. The signal flow proceeds from the aforementioned signal lines through two back-to-back tri-state buffers, the 74LS244, and then on



1. A data acquisition system achieves 50-MHz sampling with a flash converter, ECL memory and logic. The memory-mapped interface is compatible with virtually any microprocessor.



2. TTL-compatible interface logic orchestrates flow of data to and from central processor and data-acquisition system. This circuitry neatly compensates for the two-cycle delay of samples processed with a flash converter having a pipeline architecture.

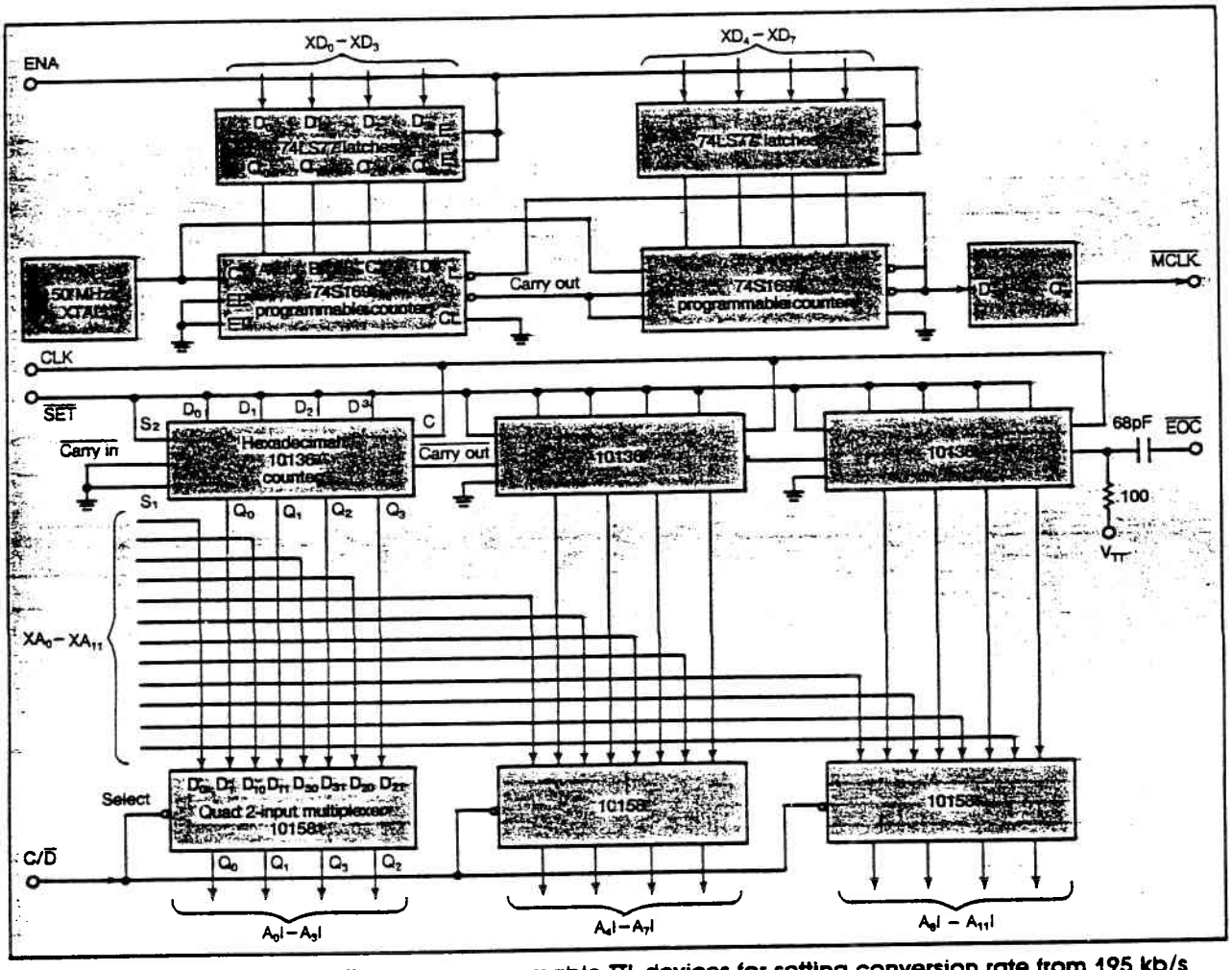
to the 10125s, which are quad MECL-to-TTL translators. From there, signal flow is to the on-board memories and to the 74LS77 clock drivers.

During the a-d conversion process, the on-board HM-2142 memories are addressed by way of 12 lines (A_0I-A_{11}I) from the system clock-and-address counter combination (Fig. 3). Like the memories, these counters are ECL devices. Keep in mind that that ECL circuits require a 100Ω pull-up resistor to V_{tt} on each output line. For clarity, the schematic of the counters, as well as all other circuits using ECL circuitry, have omitted these pull-up resistors. An additional eight address lines from the processor, A_{16}-A_{23}, are made available to the system interface block for programming the interface for a particular memory bank.

The counter frequency, and thus the conversion rate, is controlled by the central processor. More specifically, the 74LS77 latches are programmed by the processor through lines XD_0-XD_7, and are used to set the 74LS169 programmable counters. The actual conversion rate is equal to 50 MHz divided by the quantity equal to the binary setting of the latches plus 1. For example, if the latches are set to binary 5 (00000101), then the conversion rate is 50/6 MHz, or 8.333 megasamples per second. The latches can be set to a maximum value of 256 making the minimum conversion rate equal to 195.3 kilosamples per second.

The output lines from the data conversion and memory block are multiplexed by the 10158 devices. Thus, the memory can be addressed by the 10136 hexadecimal counters when a conversion is proceeding, and the processor can directly address the memory via the system data bus during periods of no activity.

Arming the interface and initiating data conversion is



3. Clock and addressing circuitry use programmable TTL devices for setting conversion rate from 195 kb/s to 8.33 Mb/s. ECL chips are used for addressing the on-board memories.

simple. First, the main processor commands the interface through the D_0-D_7 lines to set the conversion rate. The address of the controlling latches is equal to the bank address plus a string of zeros on the lower 12 address bits. After an address strobe (AS) the binary value required to realize that rate is placed in the aforementioned counter latches.

Data conversion is initiated by placing a logic 1 on the TRIG line. This command should preferably be independent of the main processor. After data conversion, an interrupt signal, EOC, indicates the end of the process. The processor then reads the stored data, and the interrupt is automatically removed.

Once a suitable interrupt has been received, the data sample is released to, or from, the processor. For this to occur, addresses xx000 to xxFFF should be specified (locations xx represents the bank address). The processor will then read or release the data, then automatically remove the interrupt.

POWER-SOURCE PARTICULARS

All ECL circuits in this system require voltages of -5.2 and -2 volts. A 5-V supply is also needed for TTL devices and from where the negative voltages are derived; and 12-V and -12-V sources to bias op amps and power transistors. In this case, the negative voltages have been obtained by applying the 5-V source to a 1403 three-terminal regulator, from which 2.5 V is obtained. That voltage is transformed to approximately -5.9 V with a 741 op amp, which after being applied to a power transistor operated as an emitter follower is transformed to a -5.2-V source that delivers the 2.5 to 3 amperes required by the system. The -12-V source is applied to the collector of the power transistor. The 2.5-V output from the regulator is also applied to an op amp and a second power transistor for the -2-V source needed by the ECL chips. □