# Efficient Hardware Realization of Frequency-Diverse Ultrasonic Flaw Detection Using Zero-Phase IIR Filters

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*Abstract*— **In this study, we address the increased computational demands of real-time ultrasonic data processing by developing an efficient frequency-diverse detection algorithm and architecture. Substantial computational savings can be obtained if the FIR filters utilized in frequency-diverse detection methods are replaced by IIR (infinite impulse response) filters. IIR filter implementations involve a much lower number of coefficients with similar filtering characteristics. However, the design of IIR filters results in phase distortion which shifts the frequency dependant signal features. This drawback greatly deteriorates the detection performance of the designed IIR bandpass filters. Consequently, for protection against phase distortion, an IIR zero-phase filter has been designed and presented. In this study, Reduced Adder Graph (RAG) algorithm is used for a hardware realization of IIR filters that does not require any dedicated multipliers. A small number of coefficients inherent to IIR filters and their multiplierless implementation provide an optimal architecture suitable for real-time ultrasonic imaging applications.**

***Keywords-Flaw detection; SSP; IIR; filtering; zero-phase***

## I. INTRODUCTION

Ultrasonic imaging has been an essential tool for nondestructive testing and flaw detection in industrial applications. Often, ultrasonic data are acquired, analyzed and processed offline. Recently, there has been an increasing demand for the realization of real-time, online applications of ultrasonic flaw detection. In this study, we aim to address the increased computational demands of real-time ultrasonic data processing by developing an efficient frequency-diverse detection algorithm and architecture. The objective of frequency-diverse ultrasonic detection is to decorrelate clutter echoes and enhance the visibility of defects. In this respect, we have analyzed the frequency-diverse ultrasonic detection methods including Fast Fourier Transform (FFT) based Split Spectrum Processing (SSP) and order statistics processors. Essentially, the SSP method is the same as applying several bandpass FIR (finite impulse response) filters. Substantial computational savings can be obtained if the FIR filters are replaced by IIR (infinite impulse response) filters which require a much lower number of coefficients with similar filtering characteristics. Our objective is to design IIR bandpass filters, and evaluate their performance in the SSP technique as an alternative. However, the design of IIR filters results in phase distortion which shifts the frequency dependant signal features. This drawback greatly deteriorates the detection performance of the designed IIR bandpass filters. Consequently, for protection against phase distortion, an IIR zero-phase filter has been designed and presented. Our experimental and simulated results demonstrate that the performance of zero-phase IIR filters for flaw detection in the presence of high scattering clutter is as effective as the FFT based SSP method.

For efficient hardware synthesis of the zero-phase IIR filters, a multiplierless implementation has been developed since the hardware complexity is directly related to the multiplication process. In general, each coefficient product is either computed sequentially or in parallel on an array of multipliers. Using an array of multipliers increases the throughput; however it also increases hardware resource usage considerably. For multiplications where one input is always constant (i.e. coefficients associated with IIR filter operations), a possible hardware implementation method would be to use primitive operator graph synthesis methods. In particular, a reduced adder graph, RAG, algorithm replaces the multiplication block of the IIR filter with a directed graph structure. In this structure, only primitive operator functions; shift and addition/subtraction operations are utilized which reduces the logic substantially. Given all the filter coefficients, the algorithm searches through the table and realizes the desired filter by finding common sub-expressions among the coefficients. The outcome is a minimal number of adders for a particular IIR filter implementation. A small number of coefficients inherent to IIR filters and optimal coefficient multiplier implementation using a minimum number of adders provide an efficient architecture suitable for real-time ultrasonic imaging applications.

## II. SPLIT SPECTRUM PROCESSING

In the ultrasonic imaging of materials, an effective method of obtaining frequency diverse information is through split spectrum processing of the broadband echoes [1,2]. In Rayleigh scattering, where the signal wavelength is significantly larger than the microstructure of materials that consist of randomly distributed reflectors and grains, the detected echoes exhibit randomness in amplitude and are sensitive to shifts in the transmitted frequency. In contrast, targets are often larger in size and are less vulnerable to variation in the transmitted frequency. In general, target echoes exhibit different distributions as a function of frequency when compared with microstructure scattering. Therefore, at any given time, the outputs of bandpass filters can be represented as a random feature vector that contains information related to target and grain echoes.

The SSP procedure has several steps. The first step is data acquisition. The experimental setup for data acquisition utilizes a pulse generator to produce the electrical impulses to drive the ultrasonic transducer. The pulse receiver is used to receive the ultrasonic echoes. The received signal is then digitized and passed through several bandpass filters (see *Figure 1*) to split the spectrum into different subbands. The output signals from the subbands are then passed into a post-detection processor for target detection [1,2]. In this paper, we present the zero-phase IIR bandpass filters for subband decomposition of the signal.

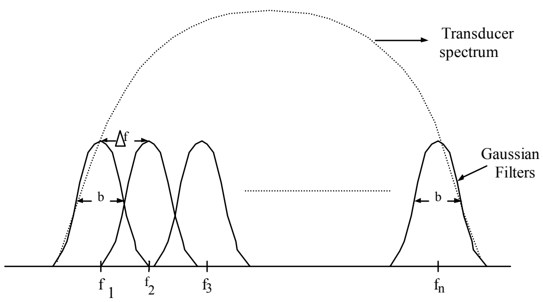


Figure 1. Bandpass filters

## III. ZERO-PHASE IIR FILTERING

IIR filters are efficient for signal decomposition, but they add random phase delays due to random nature of ultrasonic scattering echoes. Therefore, phase delays deteriorate the detection capabilities of the SSP method significantly. In order to overcome the phase-delay effect, a zero-phase IIR filter structure is used. The design of the IIR zero-phase filter is performed as follows (see *Figure 2*): first, time-reverse the discrete backscattered ultrasonic signal, then filter it with an IIR bandpass filter, time-reverse the output of the IIR bandpass filter, then filter it again by the same IIR bandpass filter. *Figure 2* shows the zero-phase IIR filtering operation steps. Analytically, it can be shown that the last output is not phase distorted. The overall transfer function of the IIR zero phase bandpass filter $H_{eq}(z)$ is obtained in terms of the IIR bandpass filter H(z) as follows:

$$H_{eq}(z) = \frac{Y(z)}{X(z)}$$

$$A(z) = X(z^{-1})$$

$$F(z) = H(z)A(z) = H(z)X(z^{-1})$$

$$B(z) = F(z^{-1}) = H(z^{-1})X(z)$$

$$Y(z) = H(z)B(z) = X(z)H(z)H(z^{-1})$$

$$H_{eq}(z) = H(z)H(z^{-1}) = |H(z)|^2$$

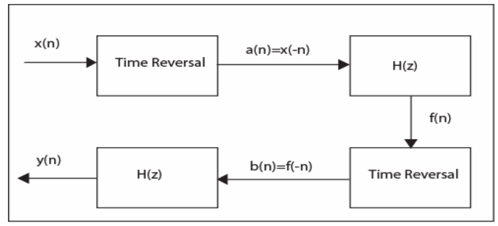


Figure 2. Zero-phase IIR filter implementation

We apply the zero-phase IIR filter to ultrasonic detection algorithm. The detection performance of IIR filters with and without zero-phase components are shown in *Table 1*. For testing, experimental A-Scans data from a steel block are acquired and analyzed. For all the measurements, the input target-to-clutter ratio is 0dB or less. It can be easily seen that the outcome of non zero-phase IIR filters do not convey any frequency related target echo information due to phase distortion. The phase distortion cancels the frequency diversity of the target echoes. On the other hand, zero-phase IIR filters perform very well with flaw-to-clutter ratio (FCR) improvement of approximately 10dB using minimization algorithm.

TABLE I. TABLE FOR PERFORMANCE COMPARISON BETWEEN NON ZERO-PHASE AND ZERO-PHASE FILTERS

| **Input data** | **FCR improvement using IIR Filtering** | | |
|---|---|---|---|
| | ***Input FCR*** | ***Non zero-phase*** | ***Zero-phase*** |
| Ascan#1 | -0.14 dB | 0.08 dB | 6.41 dB |
| Ascan#2 | -0.75 dB | -3.2 dB | 10.35 dB |
| Ascan#3 | -2.07 dB | -2.5 dB | 8.34 dB |
| Ascan#4 | -3.52 dB | -1.3 dB | 8.41dB |
| Ascan#5 | -3.74 dB | 0.5 dB | 13 dB |
| Ascan#6 | -7.26 dB | 4 dB | 9.65 dB |

In our earlier work, we have demonstrated the possible use of other frequency diverse transforms such as FFT, DCT, and WHT for ultrasonic detection algorithms [3]. Table 2 shows the performance results of these transform methods and IIR filters using the same batch of A-scan data. Again the proposed method compares very well with the previous algorithms.

TABLE II. TABLE FOR PERFORMANCE COMPARISON BETWEEN IIR BASED SSP AND OTHER METHODS SUCH AS DCT, DWT AND FFT

| **Input data** | **FCR Improvement Comparison** | | |
|---|---|---|---|
| | ***FFT*** | ***DCT*** | ***Zero-phase IIR*** |
| Ascan#1 | 10.7 dB | 8.03 dB | 6.41 dB |
| Ascan#2 | 7.21 dB | 5.31 dB | 10.35 dB |
| Ascan#3 | 14.1 dB | 14.4 dB | 8.34 dB |
| Ascan#4 | 10.17 dB | 10.77 dB | 8.41dB |
| Ascan#5 | 12.3 dB | 11.1 dB | 13 dB |
| Ascan#6 | 8.1 dB | 7.43 dB | 9.65 dB |

*Figure 3* shows a typical FCR improvement for experimental data. The flaw echoes inside the steel block are made clearly visible by suppressing the clutter echoes using zero-phase IIR filtering and SSP algorithm

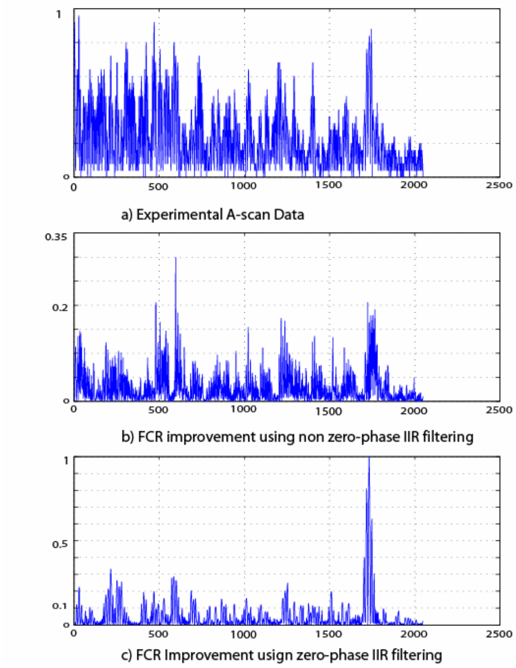


Figure 3. FCR improvement results

## IV. HARDWARE REALIZATION

Zero-phase IIR filtering has additional hardware requirements compared to SSP implementation using non-zero phase IIR filters. Another filtering operation and two time-reversal operations will be the additional hardware requirements for the zero-phase IIR implementations. It is also important to point out that after the first filtering operation, each filter output will have to be time-reversed requiring 8 time-reversal hardware. Time reversal can be realized using two buffer memories and special address generators. Although these operations increase the overall latency of the system, high clock speeds can be achieved due to regular hardware structure and sequential data flow.

The main benefit of IIR filters would be the reduced logic and power consumption compared to FIR and other transform based implementations for the SSP. Transform methods in particular are slowed down with the multiple channel inverse transforms. Fully parallel inverse transform step requires several transform engines built in to the system which are usually 1024 point or more. This would dramatically increase the hardware logic and power dissipation. In addition to inherent small filter orders, IIR filters can be realized without any dedicated multiplier blocks. Graph theory based algorithms such as Minimum Adder Graph and Reduced Adder Graph [4-5] are very convenient to use for obtaining minimal hardware usage.

IIR filters are very sensitive to integer operation and coefficient quantization due to the feedback path. Any overflow and rounding error gets augmented and filter performance deteriorates by unstable operations. In this study, IIR filter structures which are more resilient to quantization errors and also suitable for multiplierless algorithms are examined.

For fixed point IIR implementations, higher order filters are factorized in terms 2nd order filters and implemented by either cascade or parallel structures. Using small filters keeps the error of fixed point operations minimal. Parallel realization of the filters is desired since the cascade implementation is not efficient for RAG algorithm. *Figure 4* shows parallel implementation of 4th order filter using two 2nd order filters.

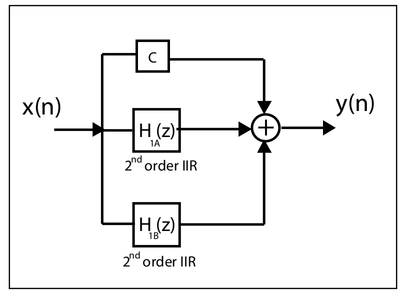


Figure 4. Parallel implementation of 4th order filter

For the multiplierless SSP implementation, all the 2nd order IIR filters are realized with Direct Form I transposed structure. The primary advantage of transposed structure is the fact that a common signal input is multiplied simultaneously by several constant coefficients during the filtering operation. This is in contrast to the normal direct form filter architectures, where constant coefficient multiplication is applied to different input samples. Therefore, by using the RAG algorithm, transposed filter architecture provides multiple uses of repeated coefficients and the multiplication block can be easily implemented with minimal logic with no dedicated multipliers. RAG algorithm makes use of the factorization of the constant coefficients. For a transposed IIR filter, it is more than likely that all the coefficients have several factors in common. *Figure 5* shows the multiplier block utilized for realizing the 2nd order IIR filter.

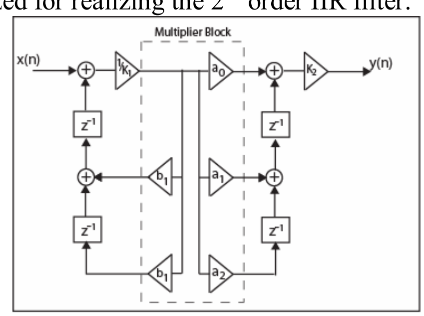


Figure 5. 2nd Order IIR filter using multiplier blocks. Direct Form– I Transposed structure

RAG algorithm replaces the multiplication block of the filter with a directed graph structure [4]. In this structure, only primitive operator functions shift and addition/subtraction operations are allowed. Multiplication by a constant integer can be described in terms of graph as follows. The initial vertex of the graph is assigned the value 1 and it receives the input samples. The terminal vertex of the graph gives the value of the multiplication result. Each vertex of the graph except the initial vertex represents an adder or a subtractor, which has two inputs, and can have any number of outputs. Each edge of the graph can be assigned a value of (±1,2,4,8...) representing multiplication of the value of the initial vertex of that edge by a value which can be implemented as a binary shift. Adders and subtractors are equal cost. Therefore, there is no difference in using positive and negative values. *Figure 6* shows $45x\psi$computed by two adders and two shift operations.

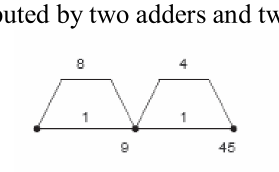


Figure 6. Multiplication with constant 45 using RAG algorithm

Since the algorithm searches through all the factors of the coefficients, the shared factors and consequently the hardware reduction and optimization can be expected to be significant for the multiplier constants in a large filter realization. For the SSP realization, 8 IIR filters are used with a common input signal after time-reversal of the input. Therefore the optimization is even more emphasized. A global multiplier block can be used and all the coefficients belonging to these filters can be implemented by exploiting the common elements. *Figure 7* shows the system architecture and the multiplier block which can implement all the constant coefficient multiplications for eight filters. Eight separate multiplier blocks are used for the second IIR filtering step since the inputs are not common.

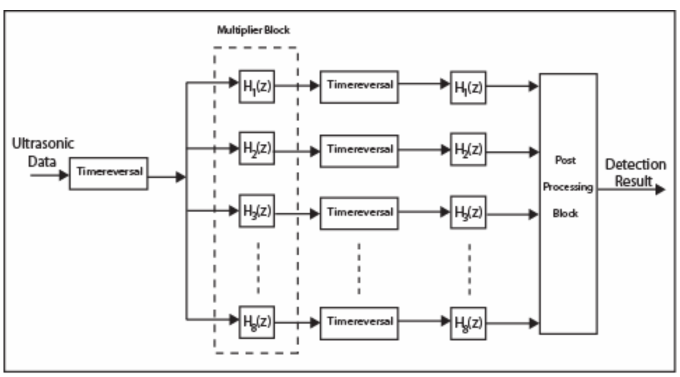


Figure 7. SSP using zero-phase IIR filters

For the results presented in *Table I*, 4th order IIR filters are used. The bandwidth of the filters is 3 MHz, and the center frequencies of the filters are shifted 0.3 MHz compared to the preceding filter. Therefore, eight filters span a frequency range 5.4 MHz in order to extract target echo information from frequency spectrum of the transducer. Chebyshev-I type IIR filters have been used to generate coefficients with the required specifications. These coefficients are then quantized for integer values by scaling with Gain factors $K_1$ and $K_2$. *RAG* algorithm generates the multiplier block architectures for the resulting coefficients.

An example of the 4th order parallel IIR filter implementation can be seen in *Figure 8.* The coefficients are quantized to integers as 6, 11, 14, 106, 126, 228, 254. The total number of adders/subtractors for coefficient multiplication for this filter is 7. This should be compared to 8 multipliers necessary for conventional fully parallel implementation. This result indicates that SSP implementation enables crucial improvements on the area and power requirements.

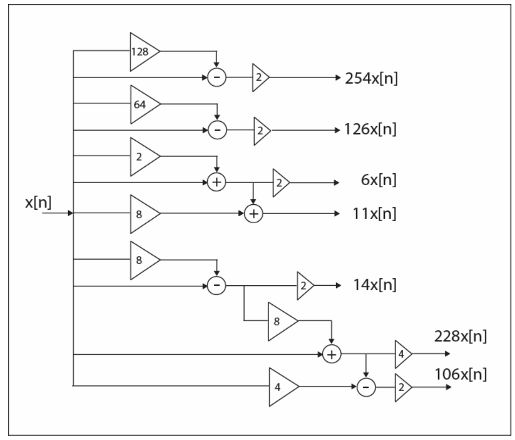


Figure 8. Realization of an 4th order parallel IIR filter with RAG algorithm

## V. CONCLUSION

In this work, it has been shown that IIR filters can be used for ultrasonic target detection applications provided that zero-phase design is integrated. For multiplierless implementation, RAG algorithm can be used if the filter structures are in parallel and transposed form. The detection performance results compare favorably with the existing methods while the hardware requirements are significantly reduced. Therefore, it can be said that IIR filter based split spectrum processing architectures are good candidates for integration in small, portable devices that can be used in real-time ultrasonic detection applications.

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