

# Chirplet Transform Signal Decomposition for Echo Detection and Estimation

Logan Sorenson, Yufeng Lu, Fernando Martinez-Vallina, and Jafar Sanjie  
 Department of Electrical and Computer Engineering  
 Illinois Institute of Technology  
 Chicago, Illinois

**Abstract**—Decomposition and analysis of nonstationary signals is a challenging problem common to radar, sonar, EEG, speech processing, and ultrasound. The Chirplet Transform Signal Decomposition (CTSD) algorithm described in this work presents a computationally efficient method for separating overlapping echoes through successive detection. Performance of this algorithm is evaluated for different signals typical in ultrasound and target detection and ranging. As part of algorithm characterization, a System on a Chip (SoC) hardware implementation has been developed.

## I. INTRODUCTION

In various signal processing applications, such as radar, sonar, EEG, speech processing, and ultrasound, the signals encountered are often nonstationary and contain highly-overlapped echoes, making detection and estimation of individual echoes problematic [1]. Therefore, signal modeling and parameter estimation of these types of signals is critical for applications involving target detection and localization, velocity measurement of moving targets, ranging systems, object recognition, deconvolution, and data compression. The nonstationary behavior of the signals can be fully captured by the Gaussian-shaped chirplet model, which has six degrees of freedom given by the parameters of time of arrival, center frequency, bandwidth factor, chirp rate, amplitude, and phase. The levels of freedom provided by the chirplet model allow a high degree of matching when decomposing a signal into constituent chirplets. It accounts for a wide variety of echoes, including those with symmetric or skewed, narrow or broad-band, and dispersive or non-dispersive characteristics. Moreover, these parameters are also closely related to physical properties of the system, such as position and velocity of a target in radar, grain size and orientation in nondestructive ultrasonic evaluation, or the path of propagation in seismology. In our previous work, [1], [2], the development of the algorithm, known as Chirplet Transform Signal Decomposition (CTSD), is discussed. This paper presents an analysis of the CTSD algorithm in decomposing a signal containing multiple interfering echoes into individual chirplet-based echoes through the use of the Chirplet Transform (CT) [3]. Furthermore, an embedded System on a Chip (SoC) running on an FPGA has been developed to test the practicality of the algorithm.

## II. CHIRPLET TRANSFORM AND SIGNAL DECOMPOSITION

In most application cases, a single chirped echo can be modeled by the Gaussian-shaped chirplet

$$f_{\Theta}(t) = \beta e^{-\alpha_1(t-\tau)^2 + i2\pi f_c(t-\tau) + i\phi + i\alpha_2(t-\tau)^2} \quad (1)$$

where  $\Theta = [\alpha_1, \alpha_2, \tau, f_c, \beta, \phi]$  denotes the parameter vector in which  $\alpha_1$  is the bandwidth factor,  $\alpha_2$  is the chirp rate,  $\beta$  is the amplitude,  $f_c$  is the center frequency,  $\phi$  is the phase, and  $\tau$  is the time of arrival. A typical chirplet signal is plotted in Figure 1.

The CT of a signal  $f_{\Theta}(t)$  is defined as

$$CT(\hat{\Theta}) = \int_{-\infty}^{\infty} f_{\Theta}(t) \Psi_{\hat{\Theta}}^*(t) dt \quad (2)$$

It represents the correlation result of the signal  $f_{\Theta}(t)$  with chirplet kernel  $\Psi_{\hat{\Theta}}$ . The kernel,  $\Psi_{\hat{\Theta}}$ , is defined as

$$\Psi_{\hat{\Theta}}(t) = \eta e^{-\gamma_1(t-b)^2 + i\omega_0 \frac{(t-b)}{a} + i\theta + i\gamma_2(t-b)^2} \quad (3)$$

where  $\hat{\Theta} = [\gamma_1, \gamma_2, \eta, \frac{\omega_0}{2\pi a}, \theta, b]$  denotes the parameter vector. The parameter  $\eta$  is set equal to  $(\frac{2\gamma_1}{\pi})^{\frac{1}{4}}$  in order to normalize the kernel.

Any signal,  $s(t)$ , no matter how complex, can be decomposed into the linear summation of multiple chirplet echoes:

$$s(t) = \sum_{j=0}^{N-1} f_{\Theta_j}(t) \quad (4)$$

where  $f_{\Theta_j}(t)$  represents the  $j^{th}$  echo and  $\Theta_j$  is the parameter vector defining  $f_{\Theta_j}(t)$ . The CTSD algorithm can recursively estimate and reconstruct chirplet echoes in the signal. The CT gives a time-frequency representation of a signal and the maximum similarity can be used to estimate the parameter vectors. The peak of the CT immediately gives the time of arrival,  $\tau$ , and the center frequency,  $f_c$ , of the dominant echo. Moreover, these two parameters can be found without reliance on the remaining parameters of the echo. The CT representation can also be used to window the original signal in time and frequency centered on the dominant echo. Knowledge of  $\tau$  and  $f_c$  obtained in the CT domain forms the basis of a successive parameter estimation technique

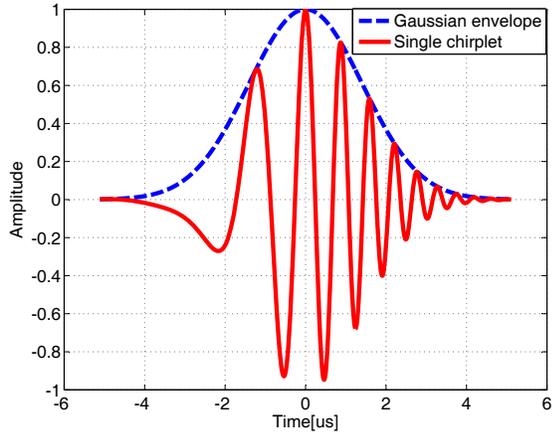


Fig. 1. A Gaussian-shaped chirplet

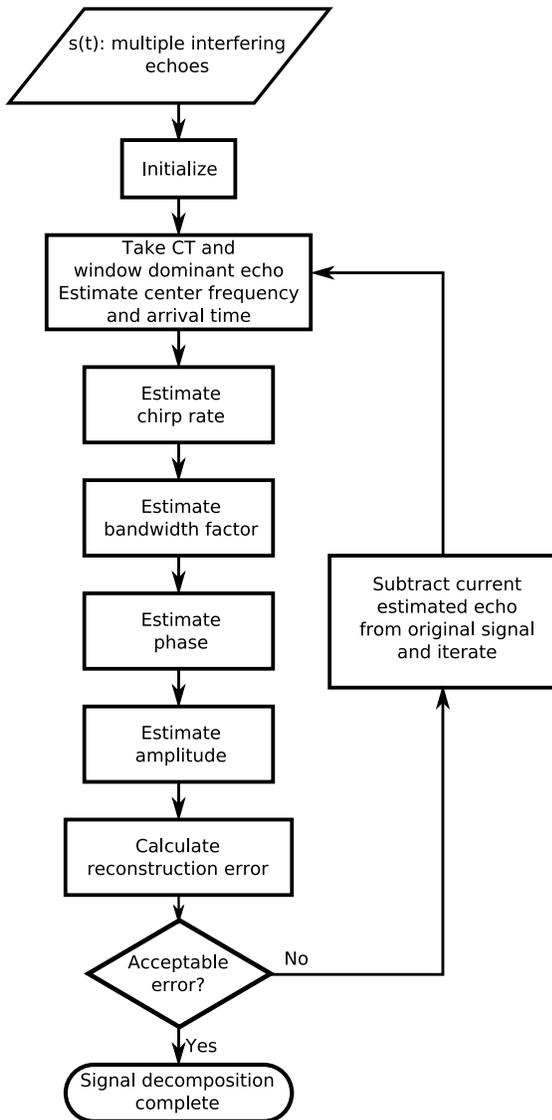


Fig. 2. Flowchart of the CTSD algorithm

for estimating the remaining parameters of the dominant echo. It has been shown in [1] that performing the parameter estimations in the order  $\alpha_2$ ,  $\alpha_1$ ,  $\phi$ , and  $\beta$  simplifies the required correlation for estimation to one dimension. In this manner, an iterative approach can be taken to decompose the complex original signal into a linear sum of individual chirplets characterized by their parameter vectors. These parameter vectors are used in combination with the chirplet equation to produce a high-fidelity representation of the original signal.

A flowchart summarizing CTSD is given in Figure 2. The signal decomposition is performed as follows. First, the signal is normalized during the initialization phase. Then, based on the chirplet transform of the signal, the most dominant echo is detected, its arrival time and center frequency determined, and the signal is windowed in time and frequency for successive parameter estimation through correlation with itself and the chirplet model. The reconstruction error is used as the termination condition of the algorithm. If the reconstruction error is below a pre-determined acceptable value, the decomposition is considered complete. Otherwise, the algorithm will loop, subtracting the dominant echo and continuing with the next most dominant echo in the residual signal. At the end of the algorithm, since the chirplet equation is known, only the set of parameter vectors of the individual chirplets are needed to reconstruct the signal. This results in high data compression while maintaining high fidelity to the original signal.

From a computational complexity standpoint, the Chirplet Transform itself requires  $O(n^2)$  operations since it is a time-frequency representation. The exact size of the time-frequency matrix depends on the sampling frequency used to capture the original signal. In the successive parameter estimation stage, each parameter is estimated through maximizing the correlation between windowed signal and chirplet kernel. Again, the accuracy is dependent on the step size used to estimate the parameters.

### III. HARDWARE IMPLEMENTATION

CTSD has been implemented as a System on a Chip (SoC) based on a Xilinx Virtex II Pro FPGA to further probe its suitability for embedded hardware. The FPGA was chosen due to its flexibility to add custom hardware to accelerate software bottlenecks. It also sped the design process by allowing in-platform testing and debugging of the system.

First, the C implementation of the algorithm was profiled to isolate which parts of the algorithm consumed the most execution time. The profile results are shown in Figure 3. As expected, the majority of time was spent in the chirplet transform and successive parameter estimation stages of the algorithm. Further analysis showed that the Fast Fourier Transform (FFT) and trigonometric functions, which are used heavily in calculating the transform and reconstructing the

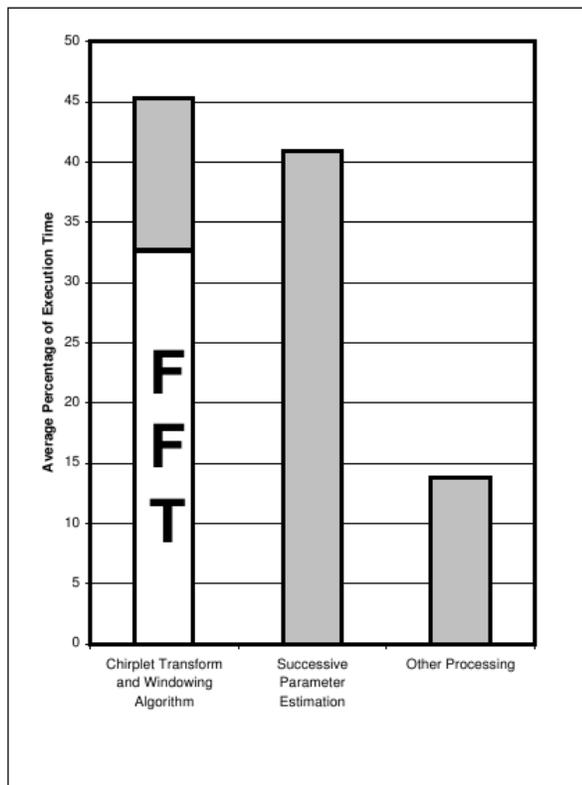


Fig. 3. Software profile results

signal, were prime candidates for hardware acceleration. A radix-4 butterfly core was selected for the FFT [4], and a CORDIC core was selected for calculating sine and cosine [5]. The CORDIC core gives the advantage of calculating both sine and cosine concurrently.

An architectural overview of the system developed in this work is shown in Figure 4. In this figure, it can be seen that this system consists of an analog sensor (an ultrasonic transducer and receiver), an A/D converter to sample and digitize the data, and two FPGAs: a pre-processor and the application processor. The pre-processing FPGA manages queuing and synchronization of the data for the application FPGA. In the application FPGA, two softcore MicroBlaze (MB) processors are used to implement both the user application and support services needed by the system [6]. As shown in Figure 4, processor 0 performs the data processing, while processor 1 provides user interaction. To obtain an efficient realization, the software algorithm was analyzed and profiled. The custom hardware accelerator cores, as chosen through the software profile, use two dedicated MicroBlaze FSL buses for high-speed data input and output [7]. Processor 1 is the master to processor 0, with FSL links to pass supervisory commands and fetch processed data. Processor 1 also manages peripherals, allowing the slave processor to operate without major interruptions. The current

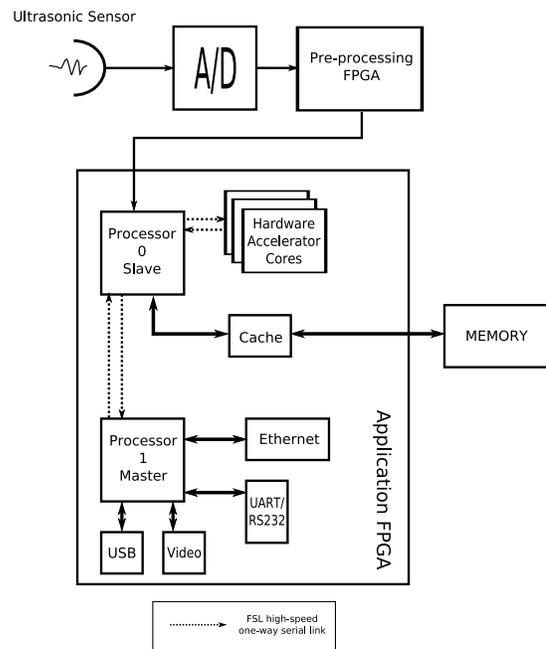


Fig. 4. Architectural overview

system offers several methods for distributing the processed data. These methods are UART, VGA, USB, and ethernet controllers. The UART is used for providing an interface to a host computer, allowing user interaction with the system and facilitating data transfer. The VGA core produces a stand-alone real-time display. The USB and ethernet facilitates exporting the data for use and analysis on other systems.

#### IV. EXPERIMENTAL RESULTS

Figure 5 shows the results of running a simulated ultrasonic signal consisting of four interfering ultrasonic echoes of different frequencies through our test system. The parameter vectors were transferred to our host computer through the UART. The individual echoes were reconstructed from the parameter vectors exported from the embedded system in MATLAB. They were then summed to produce the final reconstructed signal. The horizontal axis measures time and the vertical axis measures normalized signal intensity. The solid curve represents the original signal and the dashed curve represents the reconstructed signal. These results show that the reconstructed signal demonstrates high fidelity to the original signal. Also, the FPGA system results matched the results obtained from a MATLAB model of the algorithm, proving the feasibility of constructing an embedded implementation of the algorithm.

Figure 6 shows the results of running actual ultrasonic measurements through the system. Again, despite the extreme

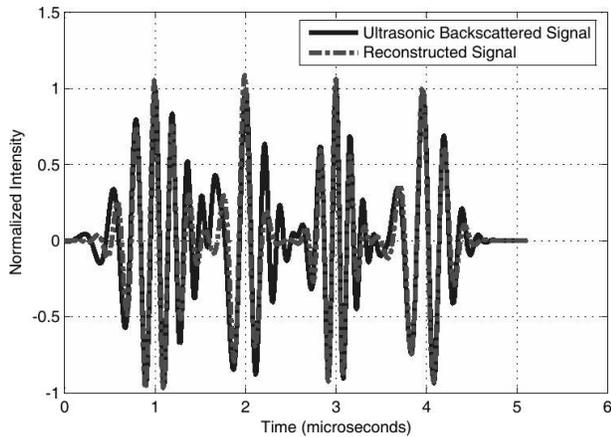


Fig. 5. Results of simulated ultrasonic signal

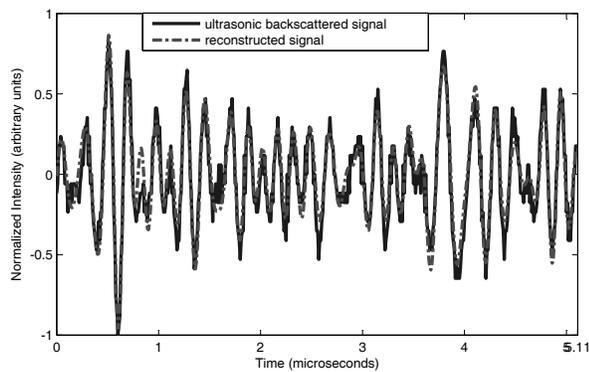


Fig. 6. Results of running experimental ultrasonic data through CTSD system

complexity of the input signal (overlapping echoes in time and frequency), CTSD performs well and achieves nearly perfect matching.

## V. CONCLUSION

This work demonstrates an embedded FPGA-based DSP system for detection and estimation using the CTSD algorithm. The developed system has been functionally verified through the use of ultrasonic measurements from an imaging application. In this application, the CTSD algorithm performs well at isolating individual echoes in the noisy environment. Furthermore, this platform can be quickly targeted to other applications in radar and sonar.

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