Real-Time FPGA Implementation of a Reconfigurable Ultrasonic Detection System

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***Abstract*- In this paper, we present hardware realization of a Reconfigurable Ultrasonic Flaw Detection system (RUFD) for real-time applications. It can be utilized in diverse environments and applications due to the run-time reconfiguration capability based on the parameters of the ultrasonic transceiver and the target material. Furthermore, this paper presents FPGA implementation results and discusses the steps for optimizing and enhancing the system in terms of the device resources usage and ultimately instrument production cost.**

I. INTRODUCTION

Ultrasonic flaw detection has real-life applications ranging from manufacturing to maintenance of materials in different industries. The presence of high scattering noise (clutter) in ultrasonic flaw detection applications induces a significant challenge. Furthermore, real-time operational requirements increase the computational complexity as well as the communication bandwidth that would result from the real-time data acquisition, signal processing, data storage and display of the results.

In this study, we present a novel configurable system architecture which can address the real-time requirements of Ultrasonic flaw detection. Flexibility of this system comes from the fact that system can be configured at run-time through the communication channels connecting the system to a host computer. These communication channels developed through a layered API gives the user the means to control and configure the system and the ability to return the data from the system back to the host computer for display and further analysis such as detection of the flaw or surface for three dimensional imaging of the target material.

Common flaw/target detection algorithms solely depend on the fact that clutter echoes in target materials exhibit randomness and are more sensitive to different frequencies in comparison with the flaw echoes [1-3]. Using this concept, algorithms such as Split-Spectrum Processing (SSP) can be used to distinguish the flaw echoes from the clutter echoes by studying the echoes in different narrow frequency bands [4-5]. This algorithm, as displayed in Fig. 1, divides the received wide-band signal from the ultrasound receiver into pre-configured sub-bands, hence differentiating and displaying the signals' distinct Flaw-to-Clutter Ratios (FCR). Ultimately these narrow-band signals reunite through a post-processing step. The algorithm used for this recombination of the narrow-bands is the absolute-minimization algorithm of the normalized narrow-band signals which results in a near optimum FCR enhancement in the processed results.

SSP algorithm is sensitive to the selection of the narrow-band filters. Hence, it necessitates a run-time reconfigurable architecture since different instruments, materials and environments require new set of parameters to make the frequency bands suitable to that specific application.

The computation and hardware resources required for each narrow-band filter limits the number of the available narrow-bands since production cost as an ASIC or FPGA implementation is directly proportional to number of these narrow-band filters. By examining the technique in Fig. 1, we can see the redundancy of the inverse FFT modules in the system which can be removed by considering an alternative sequential technique. This sequential technique eliminates all but one of the IFFT modules by time-multiplexing the inverse FFT operations.

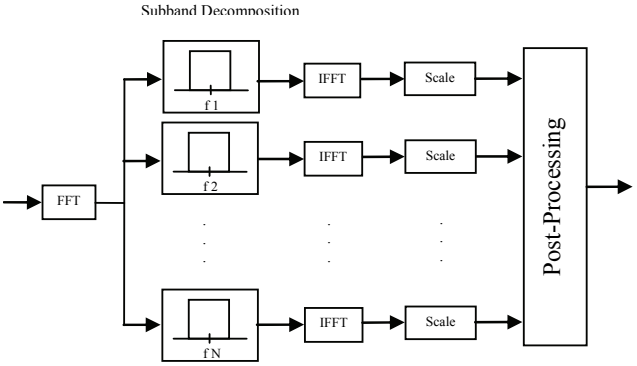

Fig. 1. Split-Spectrum Processing.

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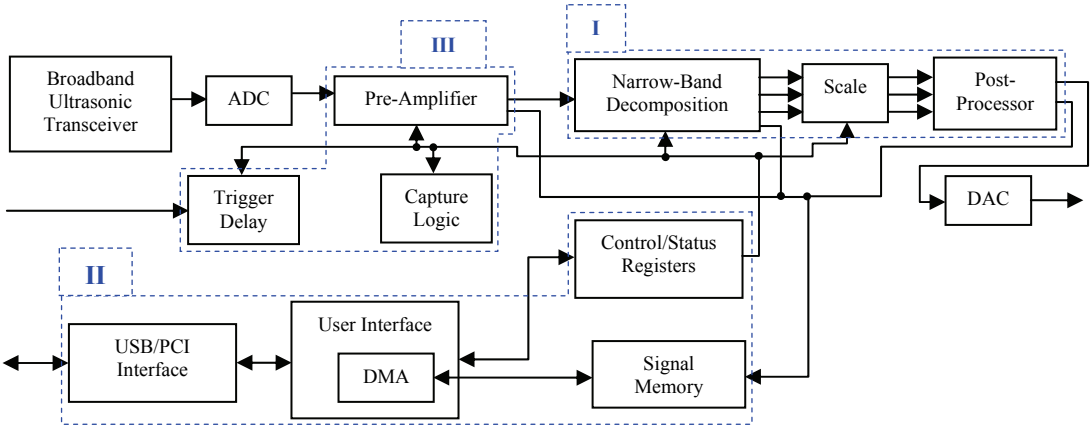

Fig. 2. System Architecture for a Real-Time Ultrasonics Detection System

The drawback of the method is the reduction in the system throughput and system refresh rate. However, it will be shown that the resulting system is still sufficient for real-time flaw detection applications.

II. System Implementation

A. Hardware Realization

The system presented in this paper was implemented in hardware as a prototype using a Xilinx Virtex-4 FPGA [6, 7] board. Considering our ultrasonic transducer frequency response range of 10 MHz, Analog-to-Digital conversion was clocked at 100 MHz which is more than adequate for this experiment. Essential hardware components of the real-time flaw detection system are presented in Fig. 2. The system includes three major assemblies of modules:

I. Ultrasonic flaw detection modules
II. Communication modules
III. Control modules

The ultrasonic flaw detection modules are a collection of components implementing the SSP technique based on a pre-configured narrow-band parameters and scaling factors. Fig. 1 displays the details of what is included in these modules.

The communication modules provide two-way communication channels to the host-computer. There are two types of communication between the RUFD system and the host-computer: Register Access (RA) and Memory Block Access (MBA). The ability to reconfigure system at run-time is due to the ability to manipulate the control registers through Register Access. There are also sets of Status Registers providing status of different modules to the host-computer. The signals in different phase of the detection process are captured into an on-chip memory block which is also transferable to the host-computer through the Memory Block Access. The MBA was implemented to overcome the communication speed burden. It contains a 16-channel DMA module providing fast access to each signal block.

Control modules provide the control signals to the whole system in addition to their 3 important functionalities: Pre-Amplification, Trigger Delay, and Signal Capturing. Pre-Amplifier module prevents the necessity of additional instruments to make the range of the captured signal suitable for the process. This module can be set dynamically at run-time and it has the range of 0 to 36dB amplification. The Trigger Delay module allows the system to detect flaw in different depths of the target material, which is an essential part of such systems. The 3-D imaging of the target material is only possible through such technique. The real-time characteristic of the system mandates the need of capturing a snap-shot of the signals from input to output of the system. Signal Capture module is in charge of this task by providing the means for the host-computer to initiate a capture command and collecting all the signals necessary for display and additional analysis of the data at the host-computer.

B. Software Implementation

A custom software package has been developed to complement the system hardware. This software package is used to reconfigure the system as well as to monitor the real-time operation within the hardware. The software package includes a Graphical User Interface (GUI) as well as the communication Application Programming Interface (API). The software follows a layered architecture displayed in Fig. 3. This architecture allows the optimum solution for software upgrades and portability to other platforms. Considering applicability of this system to wide range of applications each employing different platform, portability of the software is not a luxury but a necessity.

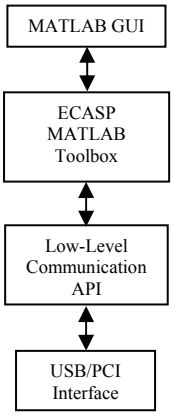

Fig. 3. Software Layers

III. Results And Discussion

Fig. 4 displays the overall configuration of the test environment used for the results given in this section. The flaw detection performance of this system was initially simulated in MATLAB, and finally implemented in hardware. The hardware implementation of the system uses 8-bit FFT/IFFT modules, and the performance of the systems in terms of the improvement in the FCR is comparable to the results from the software simulations which use 32-bit floating point representation (Fig. 5). The FCR increases by 7-9 dB using only 4 narrow-band filters which is more than adequate to bring out the flaw in the signal. Fig. 6 displays one sample of the original signal

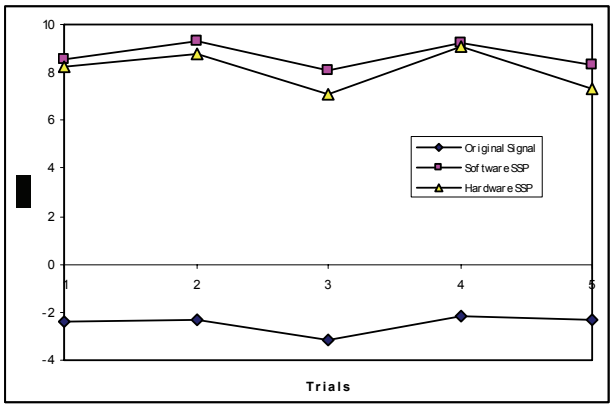

Fig. 5. Flaw-to-Clutter Ratio

with an embedded flaw and the processed signals displaying improved FCR in both software simulation and hardware results.

The system processes 1024 samples of signal at 100MHz resulting in a window of 10.2 uS which exceeds comparable systems in terms of the capacity and the speed of real-time processing. The current configuration achieves a 32.5 KHz refresh rate in the detection algorithm. This performance allows room in optimization of the system, which is the discussion of the following section.

IV. Optimization And Current Work

Although the current system achieves the initial expectations in terms of speed and the available resources in hardware, it has limitations in terms of

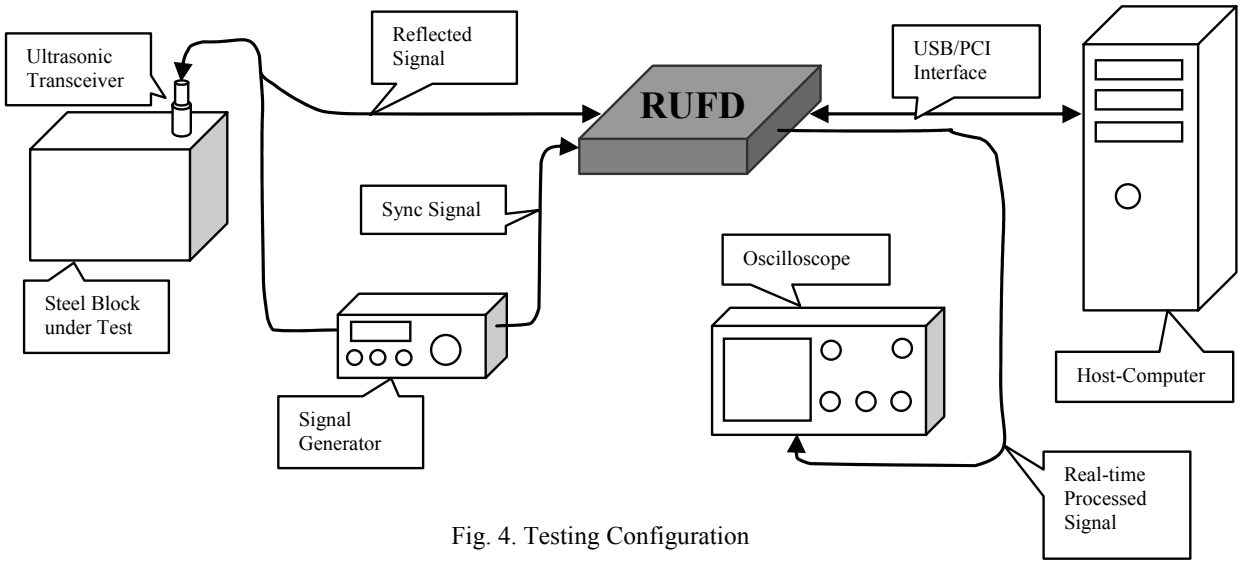

Fig. 4. Testing Configuration

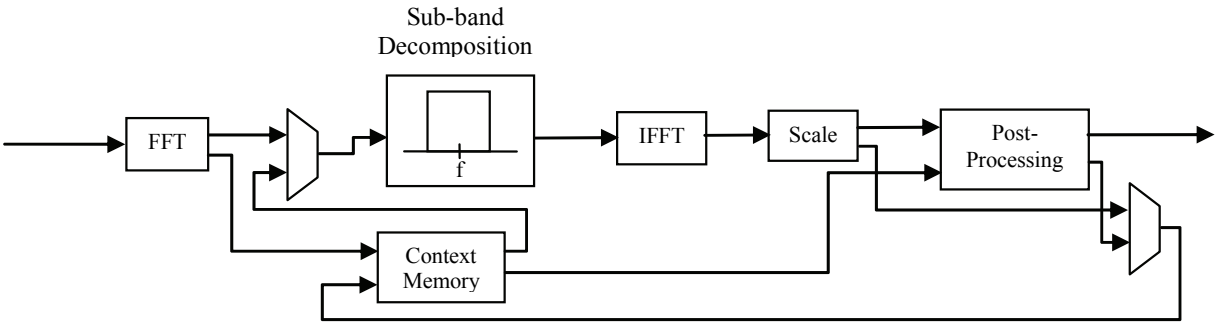

Fig. 7. Sequential Split-Spectrum Processing

the size and cost of the implementation in hardware. Examining the system blocks in the initial design, displays a redundancy in the time reversal step (IFFT) of the algorithm as well as the scaling step, which can be removed by a sequential approach.
The sequential design improves the hardware resource usage and cost.

The new SSP system (shown in Fig. 7) employs context memory and control logic to sequentially use the IFFT and Scale modules for different narrow-band decompositions resulting in removal of all but one of the modules in the system. The new design also decrease the complexity and the cost of the post-processing module, however this reduction comes with the additional cost of the new logic required for implementing the sequential approach used in the system.

The drawback of the new system is the lower throughput and refresh-rate of the system which is proportional to number of narrow-band filters configured at run-time for the SSP algorithm. The Table I lists out the new refresh rates achieved based on the number of configured narrow-bands. The detection rate although reduced stays above the initial expectation of the system. Table II compares the hardware resources used for the FPGA synthesis of each approach.

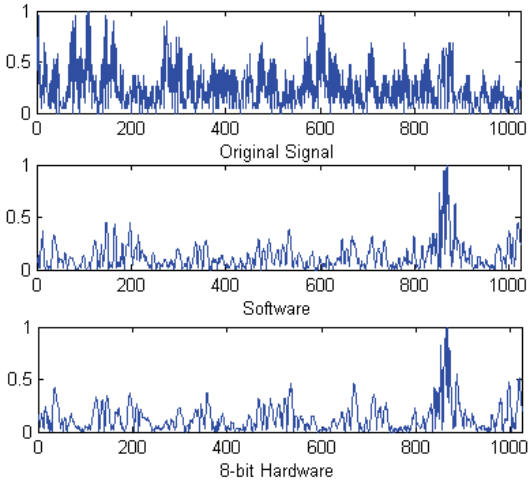

Fig. 6. Flaw Detection

The new design has decreased the usage of the required FPGA resources. This allows use of a lower-end FPGA chip (Spartan-3 [8]) costing an order of magnitude less than the original Virtex-4 FPGA, which is quite significant for the total hardware cost of the system.

V. Conclusion

In this paper a real-time reconfigurable ultrasonic flaw detection system has been presented. The well-established technique (SSP) was used in the implementation of the system. The expectations set as the requirements for the system was met after the hardware realization leaving extra space to further improvement which is the subject of our current work (Sequential Split-Spectrum Processing). This paper also compared the benefits and drawbacks of using the proposed system in terms of cost and hardware resources needed for the final system.

TABLE I
Refresh Rates

Design	# of Sub-Bands	Refresh Rate (KHz)
Parallel	4-8	32.5
Sequential	4	8
Sequential	8	4
Sequential	16	2

TABLE II
Hardware Resource Usage

HW Resources	Parallel	Sequential
DSP48's	60	24
Memory Blocks	33	18
Logic Slices	67%	27%
Logic/Mem. Slices	38%	15%

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