

Correspondence

Hardware-Efficient Realization of a Real-Time Ultrasonic Target Detection System Using IIR Filters

Erdal Oruklu and Jafar Saniie

Abstract—In this study, we address the increased computational demands of a frequency-diverse ultrasonic target detection system by developing a zero-phase IIR (ZP-IIR) filter. Several ZP-IIR filter types including Chebyshev-I, Chebyshev-II, and Butterworth were analyzed for their detection performance. The 4th-order filters with 8-bit quantized coefficients are shown to improve the flaw-to-clutter ratio by approximately 10 dB. Furthermore, the reduced adder graph algorithm is used for a hardware realization of ZP-IIR filters that does not require any dedicated multipliers. A small number of coefficients inherent to IIR filters and their multiplierless implementation provide efficient architecture suitable for compact, real-time ultrasonic imaging devices.

I. INTRODUCTION

ULTRASONIC imaging has been an essential tool for nondestructive testing and flaw detection in industrial applications. Often, ultrasonic data are acquired, analyzed, and processed offline. Recently, there has been an increasing demand for the realization of real-time, online applications of ultrasonic flaw detection. In this study, we address the increased computational demands of real-time ultrasonic data processing by developing an efficient frequency-diverse detection algorithm and architecture. The objective of frequency-diverse ultrasonic detection is to decorrelate clutter echoes and enhance the visibility of defects. In this respect, we analyzed frequency-diverse ultrasonic detection methods, including fast Fourier transform (FFT)-based split spectrum processing (SSP) and order statistics processors. Essentially, the SSP method is the same as applying several bandpass finite impulse response (FIR) filters. Substantial computational savings can be obtained if the FIR filters are replaced by infinite impulse response (IIR) filters, which require a much lower number of coefficients with similar filtering characteristics. Our objective is to design IIR bandpass filters, and evaluate their performance in the SSP technique as an alternative. However, the design of IIR filters results in phase distortion which shifts the frequency-dependent signal features. This drawback greatly deteriorates the detection performance of the IIR bandpass filters designed. Consequently, for protection against phase distortion, a zero-phase IIR (ZP-IIR) filter was designed. Our experimental and simu-

lated results demonstrate that the performance of ZP-IIR filters for flaw detection in the presence of high scattering clutter is as effective as the FFT-based SSP method.

For efficient hardware synthesis of the ZP-IIR filters, a multiplierless implementation was developed because the hardware complexity is directly related to the multiplication process. In general, each coefficient product is computed either sequentially or in parallel on an array of multipliers. Using an array of multipliers increases the throughput; however, it also increases hardware resource usage considerably. For multiplications where one input is always constant (e.g., coefficients associated with IIR filter operations), a possible hardware implementation method is to use primitive operator graph synthesis methods. In particular, a reduced adder graph (RAG) algorithm replaces the multiplication block of the IIR filter with a directed graph structure. Within this graph structure, only shift and addition/subtraction operations are utilized which reduces the logic substantially. Given all of the filter coefficients, the algorithm searches through the table and realizes the desired filter by finding common subexpressions among the coefficients. The outcome is a minimal number of adders for a particular IIR filter implementation. A small number of coefficients inherent to IIR filters and constant coefficient multiplier implementation using a minimum number of adders provide an efficient architecture suitable for compact, real-time ultrasonic imaging devices.

II. BACKGROUND

A. Split Spectrum Processing

In the ultrasonic imaging of materials, an effective method of obtaining frequency diverse information is through split spectrum processing of the broadband echoes [1], [2]. The exploration of the frequency content of ultrasonic backscattered signals can give spectral energy profiles corresponding to the grains and the larger geometric reflectors (i.e., defects). The energy loss of ultrasonic signals is caused by the microstructure of the propagating media through which scattering and absorption occurs [3]. In Rayleigh scattering, where the signal wavelength is significantly larger than the microstructure of materials that consist of randomly distributed reflectors and grains, the detected echoes exhibit randomness in amplitude and are sensitive to shifts in the transmitted frequency [4]. In contrast, targets are often larger in size and their amplitudes are less vulnerable to variation in the transmitted frequency. Because the clutter echoes are more sensitive to the frequency shifts, it is less likely that these clutter echoes contribute to the same spatial position in all of the frequency bands. Therefore, any echo signal that

Manuscript received April 12, 2008; accepted January 22, 2009.

The authors are with the Electrical and Computer Engineering Department, Illinois Institute of Technology, Chicago, IL 60616 (e-mail: erdal@ece.iit.edu).

Digital Object Identifier 10.1109/TUFFC.2009.1168

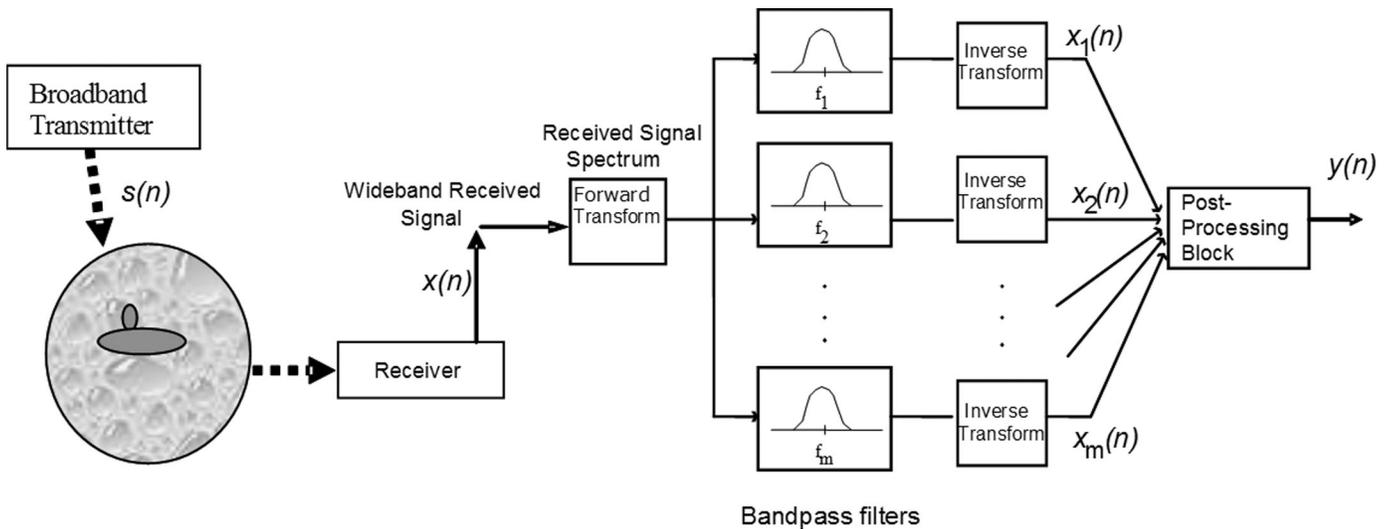


Fig. 1. Split spectrum processing target detection system.

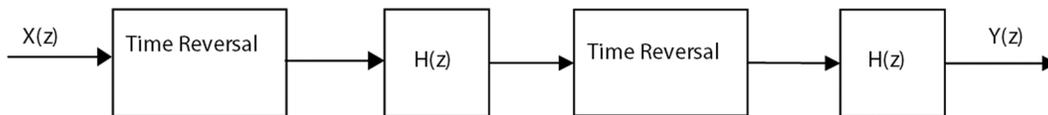


Fig. 2. Zero-phase IIR filter implementation.

is significantly large and uniformly visible among many frequency channels originates from a target echo reflector. At any given time, the output of bandpass filters can be represented as a random feature vector that contains information related to target and grain echoes.

The SSP procedure [1] has several steps, as shown in Fig. 1. The first step is data acquisition. The experimental setup for data acquisition utilizes a pulse generator to produce the electrical impulses to drive the ultrasonic transducer. The pulse receiver is used to receive the ultrasonic echoes. The received signal is then digitized and passed through a transform operation [such as FFT or discrete cosine transform (DCT)] and several bandpass filters to split the spectrum into different subbands. The output signals from the subbands are then passed into a post-processor for target detection [2], [5], [6].

It has been shown that the application of a *minimization* post-processing algorithm to frequency-diverse ultrasonic target detection works effectively [2], [5]. For the minimization algorithm, minimum amplitudes of the observation channels are obtained for each particular time: $y(n) = \min [|x_1(n)|, |x_2(n)|, \dots, |x_m(n)|]$, where $x_i(n)$ is the observation channel output corresponding to a certain frequency band.

Real-time SSP implementation is computationally intensive due to the large transform size and multichannel inverse transform operations [7]. Substantial computational savings can be obtained if the bandpass filters based on inverse and forward transforms utilized in the frequency-diverse detection methods are replaced by infinite impulse response (IIR) filters. Therefore, in this paper we present the ZP-IIR bandpass filters for subband decomposition of the signal for significantly reduced hardware complexity.

IIR filters replace the forward and inverse transform steps utilized in the SSP method.

B. ZP-IIR Filtering

IIR filters are efficient for signal decomposition, but they add random phase delays due to the nonlinear delay variation of the filters. The location of the flaw echo is shifted by a different phase term in each frequency band. Therefore, phase delays deteriorate the detection capabilities of the SSP method significantly. To overcome the phase-delay effect, a ZP-IIR filter structure is used [8]. The design of the IIR zero-phase filter is performed as follows: First, time-reverse the discrete backscattered ultrasonic signal; then filter it with an IIR bandpass filter, $H(z)$; time-reverse the output of the IIR bandpass filter; and then filter it again by the same IIR bandpass filter. Fig. 2 shows the zero-phase IIR filtering operation steps. Analytically, it can be shown that the last output is not phase distorted [8].

An important decision for zero-phase IIR filtering for the SSP method is the selection of the filter types and filter orders. This selection has implications for both the detection performance and the hardware complexity of the ultrasonic imaging system. In general, increasing the filter order size gives better frequency diverse information; therefore, the flaw-to-clutter improvement is more significant for higher-order filters.

C. Hardware Realization

The main benefit of the IIR filters is the reduced logic and power consumption compared with the FIR and other

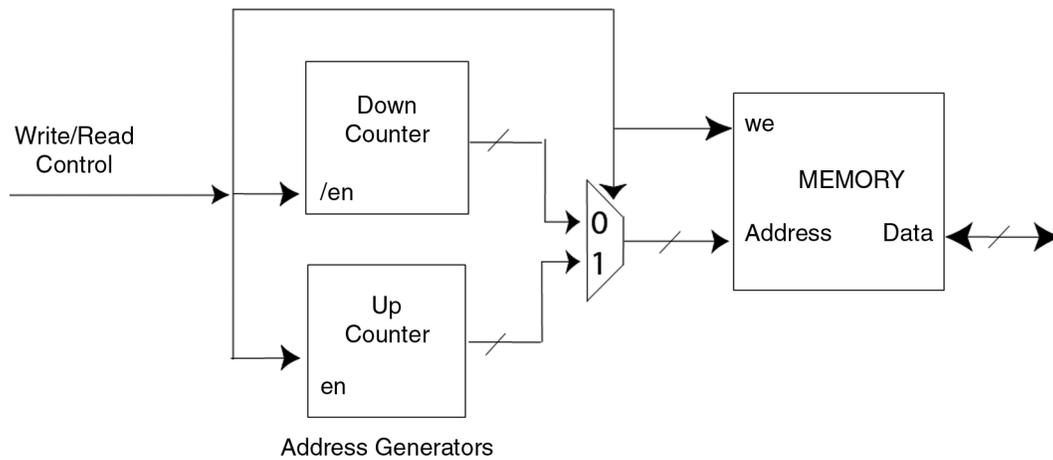


Fig. 3. Time-reversal logic.

transform-based implementations for the SSP. FIR filter implementations require higher filter orders compared with the IIR filters. Transform methods in particular are slowed down with the multiple channel inverse transforms. A fully parallel inverse transform step requires several transform engines built into the system which are usually 1024 point or more. This would dramatically increase the hardware logic and power dissipation. In addition to inherent small filter orders, IIR filters can be realized without any dedicated multiplier blocks. Graph theory-based algorithms, such as minimum adder graph and RAG [9], [10], replace the multiplication block of the filters with only primitive operator functions, such as shift and addition/subtraction operations.

For the ZP-IIR method, a second filtering operation and 2 time-reversal operations are the additional computational requirements. It is also important to point out that after the first filtering operation, each filter output has to be time-reversed, requiring multiple (i.e., the same number as number of filters) time-reversal hardware blocks. Time-reversal logic can be realized using an up/down counter for address generation, a multiplexer, and a memory that can store N words as shown in Fig. 3. When *write* mode is enabled, the up-counter is active; otherwise the down-counter is enabled for read operations. If input data are available in memory (i.e., not streaming input), the first time-reversal step can be implemented by simply generating addresses in reverse order. Otherwise additional N clock cycles are added to the overall latency of the system.

III. METHODS

A. ZP-IIR Filter Design

IIR filters are very sensitive to integer operation and coefficient quantization due to the feedback path. Any overflow and rounding error gets augmented and the filter performance deteriorates by unstable operations. In

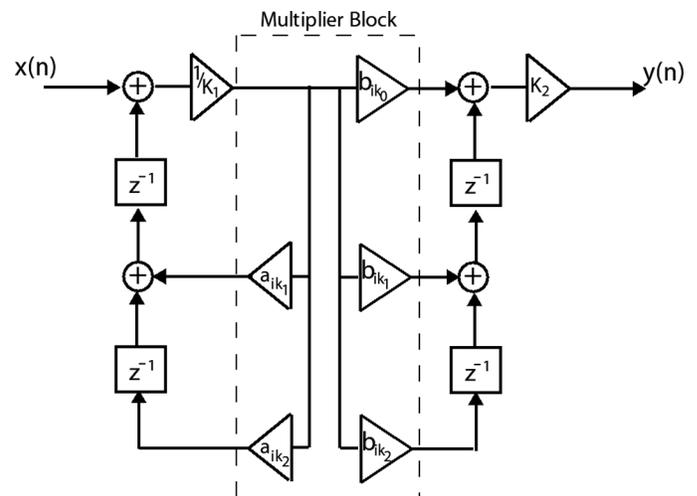


Fig. 4. Second-order IIR filter using multiplier blocks. Direct form I transposed structure.

this study, IIR filter structures that are more resilient to quantization errors and also suitable for multiplierless algorithms are examined. Therefore, for the fixed-point IIR implementations, higher-order filters are factorized in terms of 2nd-order filters and implemented by cascade structures. Using small filters keeps the error of the fixed-point operations minimal.

For multiplierless SSP implementation, all of the 2nd-order IIR filters are realized with a direct form I transposed structure. The primary advantage of the transposed structure is the fact that the RAG algorithm can be utilized to construct the necessary multiplier block because a common signal input is multiplied simultaneously by several constant coefficients during the filtering operation. This is in contrast to the normal direct form filter architectures, where constant coefficient multiplication is applied to the different input samples. Therefore, by using the RAG algorithm, the transposed filter architecture provides multiple uses of the repeated coefficients, and the multiplication block can be easily implemented with minimal logic and no dedicated multipliers. The RAG al-

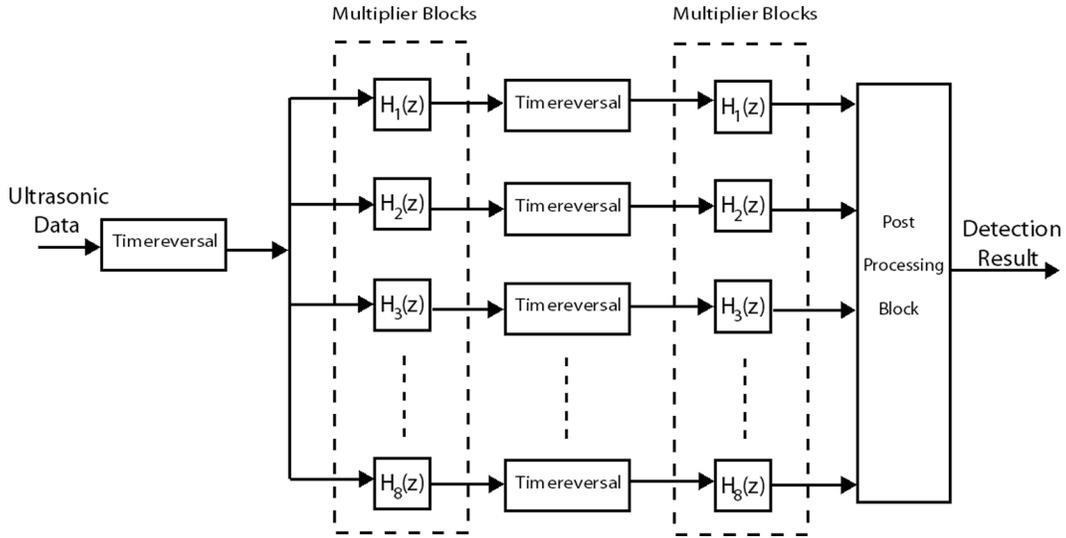


Fig. 5. SSP using zero-phase IIR filters.

TABLE I. SSP DETECTION PERFORMANCE COMPARISON BETWEEN FFT, DCT, NONZERO-PHASE IIR AND MULTIPLE ZERO-PHASE IIR FILTERING-BASED METHODS.

Filter order	Input FCR	FFT	DCT	Nonzero-phase IIR	Zero-phase IIR filters								
					Chebyshev-I			Chebyshev-II			Butterworth		
	N/A	N/A	N/A	N/A	4	6	8	4	6	8	4	6	8
Ascan#1	3.6	15.3	12.6	0.08	11.3	13.09	11.34	8.87	8.96	11.05	7.03	7.94	8.56
Ascan#2	-2.97	12.07	11.1	-3.2	12.96	11.88	10.94	12.55	13.57	11.4	10.05	10.6	10.55
Ascan#3	-6.66	14.1	12.1	-2.5	8.95	11.23	13.32	13.16	13.46	14.38	8.44	9.98	10.9
Ascan#4	-0.38	6.88	8.51	-1.3	11.98	11.58	11.37	6.78	9.27	9.89	7.48	9.07	9.57
Ascan#5	-3.74	12.3	10.2	0.5	12.31	17.02	14.18	12.25	13.47	13.85	9.49	12	12.95
Ascan#6	-2.85	10.15	9.95	4	6.82	9.6	11.32	6.75	7.65	8.47	6.61	7.55	7.99
Ascan#7	-4.19	12.67	11.3	2.1	12.36	15.5	15.5	7.27	7.58	12.17	8.89	10.72	11.55
Ascan#8	0	10.6	8.2	3.1	5.21	8.31	8.02	11.27	10.9	10.23	5.78	6.63	7.07
Ascan#9	1.64	10.7	7.1	0.22	7.1	7.6	8.55	8.69	8.76	8.44	5.57	6.45	7.08
Ascan#10	-1.20	10.5	10.1	3.3	9.85	12.69	9.89	7.4	7.49	8.38	7.42	9.1	9.64
Average FCR improvement	N/A	11.52	10.1	0.63	9.88	11.85	11.44	9.49	10.11	10.82	7.67	9.00	9.58

algorithm makes use of the factorization of the constant coefficients. For a transposed IIR filter, it is more than likely that all of the coefficients have several factors in common. Fig. 4 shows the multiplier block for realizing the 2nd-order IIR filter. The terms a_k and b_k are filter coefficients, and K_1 and K_2 are scaling coefficients for the fixed-point implementation.

Furthermore, to obtain minimal hardware requirements and robust performance, we analyzed 3 different IIR filter types: Chebyshev-I, Chebyshev-II, and Butterworth with filter orders 4, 6, and 8.

B. SSP Implementation Using ZP-IIR Filters

We apply the zero-phase IIR filters to the ultrasonic detection algorithm. Eight bandpass IIR filters are used for SSP realization to extract frequency diverse information. Fig. 5 shows the system architecture and the multiplier blocks that implement all of the constant coefficient multiplications for 16 filters. Total latency of the system is $2N$ clock cycles for N -point input data. N clock cycles

are required for the first IIR filtering pass and another N clock cycles for the second IIR filter pass after time reversal. Post-processing step minimization can be computed in-place due to parallel implementation of the filters. The total memory requirement is $9N$ words.

For comparison, in FFT-based SSP systems, parallel implementation is difficult to achieve because it requires 9 individual FFT cores (1 forward FFT and 8 inverse FFTs; see Fig. 1.) Therefore, large application-specific integrated circuit (ASIC) designs or field-programmable gate array (FPGA) devices are mandatory. Alternatively, using a single FFT core, serial implementation yields a system latency of $10N$ clock cycles (N clock cycles for forward FFT + $8N$ clock cycles for successive inverse FFTs + N clock cycles for minimization), which is significantly slower than for the ZP-IIR method.

C. Experimental Setup

For performance analysis and testing, the experimental A-scan data from a steel block (type 1018, grain size

50 μm) were acquired and analyzed. A Panametric type 5052 pulser/receiver (Panametrics, Waltham, MA) is used to drive the ultrasonic transducers and to receive the ultrasonic echoes. The received echo signals are then converted to digital data for split spectrum processing. The A-scan measurements were conducted using an Agilent 54616C digital oscilloscope (Agilent Technologies, Inc., Santa Clara, CA) and a broadband unfocused ultrasonic transducer (Panametric A3062) of 0.375-inch diameter with 5-MHz center frequency. Data were acquired with a 100-MHz sampling rate and each sample is 8 bits. The steel block has several holes (1.5-mm diameter) at known, separate locations. All of the A-scan measurements probe the hole positions within the steel block. For performance analysis, flaw-to-clutter ratio (FCR) is calculated by $\text{FCR} = 20 * \log_{10}(F/C)$, where F is the maximum flaw echo amplitude and C is the maximum clutter echo amplitude.

IV. RESULTS

Table I shows the performance results of the transform methods FFT and DCT as well as nonzero-phase (no time-reversal and second pass of IIR filtering take place) and zero-phase IIR filters using the same batch of A-scan data. It can be seen that the outcomes of nonzero-phase IIR filters do not convey any frequency-related target echo information due to the phase distortion. The phase distortion cancels the frequency diversity of the target echoes. On the other hand, zero-phase IIR filters perform very well with flaw-to-clutter ratio (FCR) improvement of approximately 10 dB using the minimization algorithm.

Table I also shows the ultrasonic detection results for various IIR filter types and orders. Among the filters, the Chebyshev-I filter achieves the most robust performance even for a 4th-order filter. It is also important to point out that the 4th-order Chebyshev-I filter has 9.88-dB average FCR improvement which is a significant clutter reduction. It is essential to integrate only small-order filters for reduced logic and power consumption in compact imaging devices. Therefore, a system-on-a-chip (SoC) architecture can be built using only 4th-order IIR filters which is capable of meeting the requirements of ultrasonic detection applications. Fig. 6 shows a typical FCR improvement for experimental ultrasonic data. The flaw echoes inside the steel block are made clearly visible by suppressing the clutter echoes using FFT, DCT, and zero-phase IIR filtering-based SSP algorithms. For all of the methods, the absolute minimization method [1] is applied to the inverse transform and filter outputs in the post-processing stage.

Table II shows the hardware realization results for a case study using FFT and ZP-IIR SSP detection methods. In both cases, 8 different frequency domain windows are used, covering the input signal frequency spectrum from 0 to 5.1 MHz. The bandwidth of a single frequency window is 3 MHz and the shift between the successive windows is 0.3 MHz. Input data size N is equal to 1024 data points.

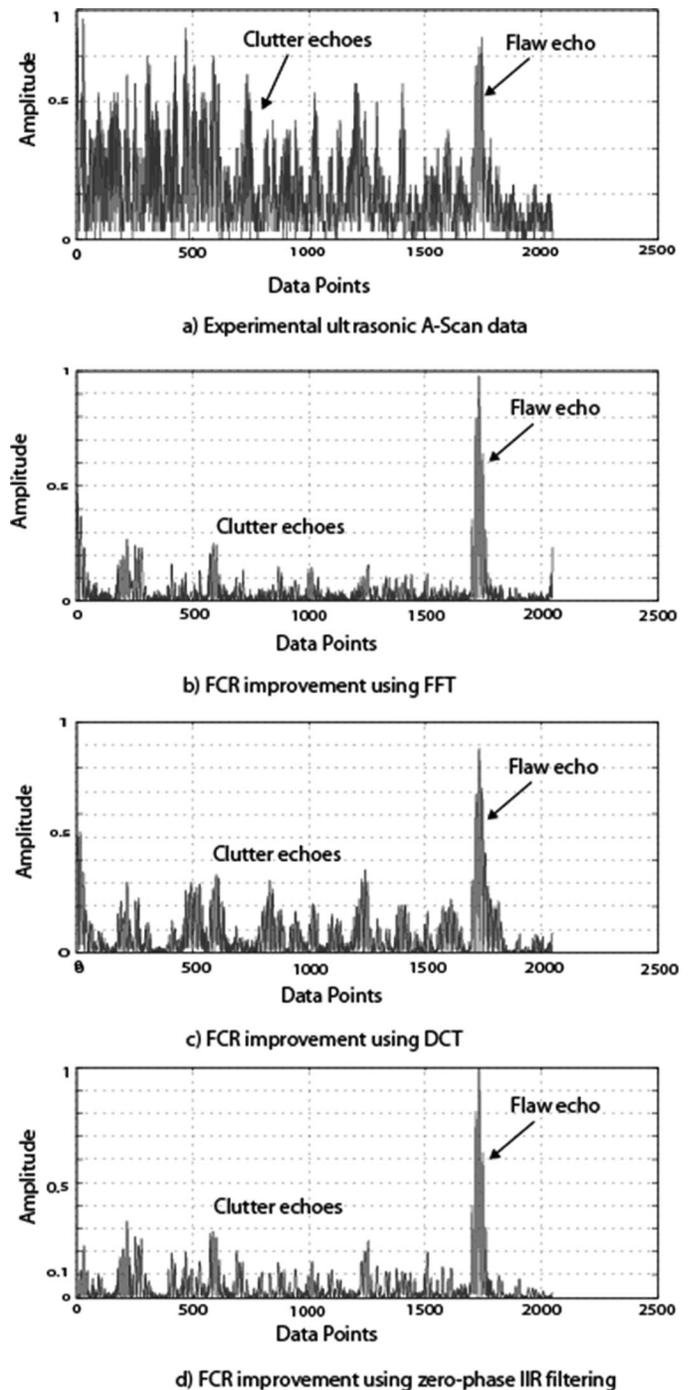


Fig. 6. Experimental ultrasonic data (a); FCR improvement using (b) FFT, (c) DCT, and (d) ZP-IIR filtering methods.

Each SSP method has been realized using Virtex-2 Pro (xc2vp30-7) FPGA devices (Xilinx, Inc., San Jose, CA) and Xilinx ISE v8.1 development tools. FFT implementation is based on Xilinx Logic-Core FFT v3.2 [11] and uses pipelined, streaming I/O architecture where the total transform clock cycles are equal to the transform size N . This FFT architecture is the fastest implementation available in this intellectual property (IP) core and is chosen to obtain similar throughput with respect to the ZP-IIR method (i.e., streaming I/O). For the ZP-IIR implementa-

TABLE II. FPGA HARDWARE UTILIZATION FOR ULTRASONIC DETECTION ALGORITHMS.

	FFT-based SSP	ZP-IIR filter-based SSP	
	Serial (1 FFT core)	With multiplication	Multiplierless using RAG
Slices	3427	8336	4541
4-Input LUTs	5158	14360	6486
Flipflops	5697	2434	2450
Block ram	6	18	26
18 × 18-Bit multipliers	22	0	0
Clock speed (MHz)	200	64	65
Latency- total clock cycles (N)	10	2	2
Total execution time for $N = 1024$ points (μs)	51.2	32	32

tion, 4th-order filters are designed. Chebyshev-I type-IIR filters were used to generate coefficients with the required specifications. These coefficients are then quantized for integer values by scaling. Table II also shows 2 types of ZP-IIR implementations: 1) using multiplication for each coefficient; and 2) using multiplierless architectures where the RAG algorithm generates the multiplier block architectures for the required coefficients. The results indicate significant reduction in hardware resource usage (50% fewer look up tables (LUT) and 40% fewer logic slices because twenty-two 18 × 18-bit multipliers are equivalent to approximately 8000 LUTs and 4000 slices in Virtex2pro FPGAs [11]) when the ZP-IIR method with multiplierless implementation is employed in ultrasonic detection algorithms. This is mainly due to the fact that small IIR filters replace the large FFT cores.

The FFT architecture is pipelined and can reach 200-MHz clock speed whereas the IIR filter-based methods are clock limited and cannot be pipelined due to the feedback loops (the current FPGA compiler is unable to optimize the feedback loops) and the predetermined FPGA architectures that rely on configurable logic blocks (CLBs). Faster clock speeds can be obtained with very large-scale integration implementations and no architectural restrictions. Furthermore, for ZP-IIR methods, parallel implementation is feasible which increases the throughput and yields a faster realization than FFT-based methods. As shown in Table II, the total time for implementing the ZP-IIR method with $N = 1024$ points through 8 filters is 1.6 times faster than that for the single FFT core-based SSP detection method. One drawback for the ZP-IIR filter implementation is the lack of flexibility because the hardware logic based on minimum adders cannot be modified for different filter specifications.

The repetition rate in ultrasonic imaging systems dictates the processing time for real-time applications. For such systems, a typical value for a repetition rate is 1000 Hz resulting in 1-ms time intervals for processing the acquired data. Fig. 7 shows the timing requirements for a typical application. Data acquisition takes approximately 10 μs (considering 1024 samples acquired at a 100-MHz sampling rate). Consequently, the target detection system has to process the data, store the results, and either dis-

TABLE III. PERFORMANCE COMPARISON BETWEEN SOFTWARE AND HARDWARE IMPLEMENTATION OF ZP-IIR FILTERS IN ULTRASONIC DETECTION SYSTEMS.

Input data	FCR improvement comparison (dB)		
	Input FCR	Real numbers	Fixed point
Ascan#1	3.6	11.3	11.62
Ascan#2	-2.97	12.96	11.95
Ascan#3	-6.66	8.95	8.61
Ascan#4	-0.38	11.98	10.10
Ascan#5	-3.74	12.31	10.87
Ascan#6	-2.85	6.82	8.2
Ascan#7	-4.19	12.36	10.32
Ascan#8	0	5.21	3.27
Ascan#9	1.64	7.1	6.18
Ascan#10	-1.20	9.85	8.75
Average FCR improvement	—	9.88	8.98

play, transmit, or store the processed results in 990 μs . An execution time of 32 μs (listed in Table II for 1024 data points) indicates that the IIR filters can be used very effectively for even more demanding applications.

To analyze the fixed-point coefficients and quantization effects, software implementation with MATLAB (The MathWorks, Inc., Natick, MA) using real numbers is compared with the hardware implementation with fixed-point numbers using a Xilinx FPGA device. The coefficients for the fixed-point IIR filters are quantized to 8-bit values. Table III shows the flaw-to-clutter improvement for both systems using 4th-order Chebyshev-I filters. It can be seen in Table III that the FCR improvement is hampered by the fixed-point operation by an average of approximately 1 dB. This is still respectable considering the minimal hardware realization requirements (i.e., 4th-order filter and 8-bit coefficients).

V. COMPARISON OF FIR AND IIR REALIZATIONS FOR SSP

There are 2 important parameters that significantly affect the computational complexity of target detection algorithms. The first parameter is the sampling rate used for ultrasonic data acquisition. The sampling rate deter-

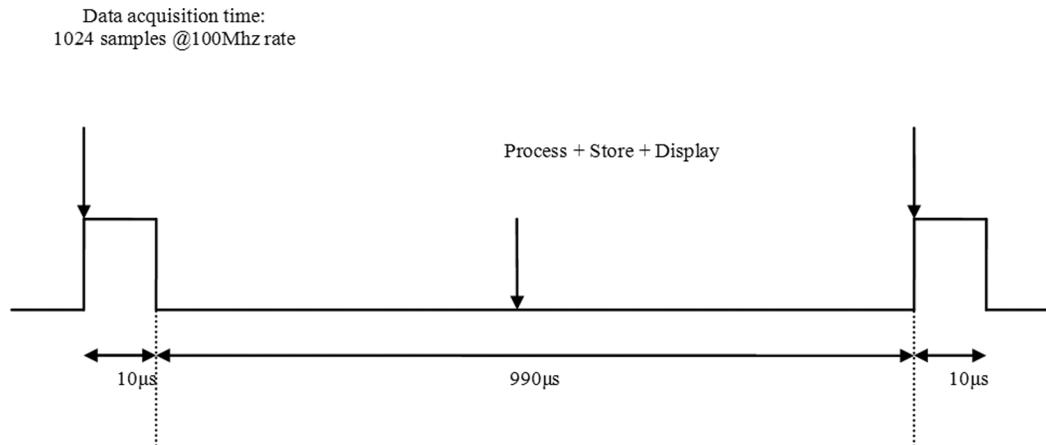


Fig. 7. Typical timing requirements.

mines the resolution of the signal, and a higher sampling rate improves the detection of a target's exact location. Lowering the sampling rate may reduce computations at the expense of SSP performance. The second parameter is the number of bandpass filter coefficients used in the SSP algorithm. For both FIR and IIR implementations, each unique coefficient indicates a multiplication operation. Hence, it is desirable to use minimum-order filters that satisfy bandpass specifications.

In this section, we compare FIR and IIR filter implementations of the SSP algorithm using 2 different sampling rates. For the 100 MHz sampling rate, it was shown in Table I that 4th-order IIR filters can achieve close to 10-dB FCR improvement. An equivalent implementation using FIR filters requires filters with more than 100 coefficients for similar FCR performance. To reduce the order of FIR filters, the sampling rate can be reduced as long as the Nyquist rate is satisfied. Table IV shows FCR results with a 20-MHz sampling rate and 24-tap FIR bandpass filters. Although this realization with 24 multiplications achieves an average of 6.45-dB FCR improvement, second-order IIR filters can achieve 6.71-dB FCR improvement with fewer multiplications (3 multiplications for each pass, resulting in 6 multiplications total) with a 20-MHz sampling rate. With this sampling rate, the computational rate is relaxed but the exact location of the flaw will be 5 times worse compared with the 100-MHz sampling rate.

VI. CONCLUSION

In this work, a dedicated architecture for the SSP implementation based on IIR filters is presented with 2 objectives: reduced logic and high throughput. It was shown that IIR filters can be used for ultrasonic target detection applications provided that zero-phase design is integrated. Two time-reversal operations and a second filtering step ensure that no-phase distortion will appear in the filtered outputs. IIR filters require small filters; it was shown that 4th-order filters can be used effectively to implement the SSP-based ultrasonic detection algorithm. Because the IIR filters are very susceptible to quantiza-

TABLE IV. PERFORMANCE COMPARISON BETWEEN FIR AND IIR FILTER IMPLEMENTATIONS WITH 20-MHZ SAMPLING RATE.

Input data	FCR improvement comparison		
	Input FCR (dB)	24th-order FIR	2nd-order IIR
Ascan#1	3.6	14.9	12.27
Ascan#2	-2.97	5.86	6.46
Ascan#3	-6.66	0.27	4.0
Ascan#4	-0.38	8.1	9.43
Ascan#5	-3.74	3.8	8.39
Ascan#6	-2.85	6.54	5.9
Ascan#7	-4.19	8.1	5.6
Ascan#8	0	7.5	6.97
Ascan#9	1.64	6.03	6.13
Ascan#10	-1.20	6.37	8.43
Average FCR improvement	—	6.45	6.71

tion effects, 2nd-order IIR filter structures are utilized in the implementation. Even 8-bit quantized coefficients are shown to have a robust detection performance. To further reduce the hardware requirements, dedicated multipliers are replaced by minimum adder blocks. For multiplier-less implementations, an RAG algorithm can be used if the filters are in direct form I-transposed structure. However, the multiplierless implementation of IIR filter blocks limits the flexibility of the architecture because changing the filter parameters would require a complete redesign of the filter structure for optimal RAG implementation. Overall, the detection performance results compare favorably with the existing methods whereas the hardware requirements are significantly reduced. Therefore, it can be said that ZP-IIR filter-based split spectrum processing architectures are good candidates for integration in small, portable devices that can be used in real-time ultrasonic target detection applications.

REFERENCES

- [1] V. L. Newhouse, N. M. Bilgutay, J. Saniie, and E. S. Furgason, "Flaw-to-grain echo enhancement by split-spectrum processing," *Ultrasonics*, vol. 20, pp. 59–68, Mar. 1982.

- [2] J. Saniie, D. T. Nagle, and K. D. Donohue, "Analysis of order statistic filters applied to ultrasonic flaw detection using split spectrum processing," *IEEE Trans. Ultrason. Ferroelectr. Freq. Control*, vol. 38, no. 2, pp. 133–140, Mar. 1991.
- [3] E. P. Papadakis, "Ultrasonic attenuation caused by scattering in polycrystalline metals," *J. Acoust. Soc. Am.*, vol. 37, pp. 711–717, 1965.
- [4] J. Saniie and D. T. Nagle, "Analysis of order statistic CFAR threshold estimators for improved ultrasonic flaw detection," *IEEE Trans. Ultrason. Ferroelectr. Freq. Control*, vol. 39, no. 5, pp. 618–630, Sep. 1992.
- [5] J. Saniie, K. D. Donohue, and N. M. Bilgutay, "Order statistic filters as post-detection processors," *IEEE Trans. Acoust. Speech Signal Process.*, vol. 38, no. 10, pp. 1722–1732, Oct. 1990.
- [6] J. Saniie, T. Wang, and X. Jin, "Performance evaluation of frequency diverse Bayesian ultrasonic flaw detection," *J. Acoust. Soc. Am.*, vol. 92, pp. 2034–2041, Apr. 1992.
- [7] E. Oruklu and J. Saniie, "High speed design and performance evaluation of frequency diverse orthogonal transforms for ultrasonic imaging applications," in *Proc. IEEE Symp. Ultrason.*, vol. 1, Oct. 2003, pp. 258–261.
- [8] E. Oruklu, F. M. Vallina, and J. Saniie, "Efficient hardware realization of frequency-diverse ultrasonic flaw detection using zero-phase IIR filters," in *Proc. IEEE Symp. Ultrason.*, vol. 3, Sep. 2005, pp. 1785–1788.
- [9] A. G. Dempster and M. D. Macleod, "Use of minimum adder multiplier blocks in FIR digital filters," *IEEE Trans. Circuits Syst. II*, vol. 42, no. 9, pp. 569–577, Sep. 1995.
- [10] A. G. Dempster and M. D. Macleod, "Comparison of fixed-point FIR digital filter design techniques," *IEEE Trans. Circuits Syst. II*, vol. 44, pp. 591–593, Jul. 1997.
- [11] Product documentation, *LogiCORE Fast Fourier Transform (FFT) v3.2*, Xilinx, Inc, San Jose, CA, Aug. 2005.