10.1109/ULTSYM.2013.0135

Performance Evaluation of FPGA based Embedded ARM Processor for Ultrasonic Imaging

Spenser Gilliland, Pramod Govindan, Thomas Gonnot and Jafar Saniie
Department of Electrical and Computer Engineering
Illinois Institute of Technology, Chicago IL, U.S.A.

Abstract- **This study evaluates the performance of an FPGA based embedded ARM processor system to implement signal processing for ultrasonic imaging and nondestructive testing applications. FPGA based embedded processors possess many advantages including a reduced overall development time, increased performance, and the ability to perform hardware-software (HW/SW) co-design. This study examines the execution performance of split spectrum processing, chirplet signal decomposition, Wigner-Ville distributions and short time Fourier transform implementations, on two embedded processing platforms: a Xilinx Virtex-5 FPGA with embedded MicroBlaze processor and a Xilinx Zynq FPGA with embedded ARM processor. Overall, the Xilinx Zynq FPGA significantly outperforms the Virtex-5 based system in software applications**

I. Introduction

Generally, ultrasonic imaging applications use personal computers or hand held devices. As these devices are not specifically designed for efficiently executing computationally intensive ultrasonic signal processing algorithms, the performance of these applications can be improved by executing the algorithms using a dedicated embedded system-on-chip (SoC) hardware. However, porting these applications onto an embedded system requires deep knowledge of the processor architecture and embedded software development tools.

In this study, a Reconfigurable Ultrasonic System-on-chip Hardware (RUSH) platform is developed to implement ultrasonic signal processing algorithms in embedded software and reconfigurable hardware. Figure 1 shows the RUSH SoC setup for ultrasonic imaging applications. The RUSH platform enables ultrasonic researchers to conduct real-time signal processing experiments for nondestructive testing and imaging applications. The RUSH platform includes a 16-bit ADC for capturing ultrasonic signals at a sampling rate up to 250 MSPS. The embedded processor executes platform independent C code within a Linux based operating system. This allows the reuse of a substantial portion of available software and reduces overall system development time. The modular design structure of RUSH platform supports an ability to improve system performance by upgrading the FPGA to a more advanced FPGA device.

In this study, we evaluate and optimize the computation time of three ultrasonic signal processing algorithms (i.e.,

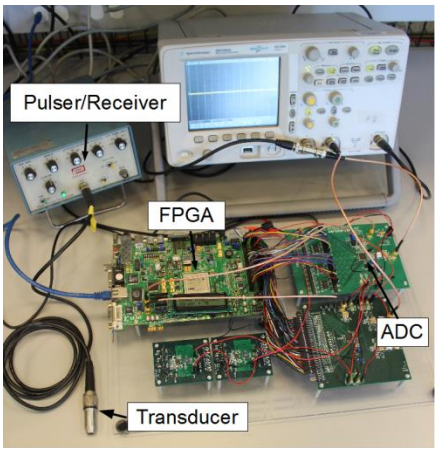

Figure 1. RUSH SoC setup

frequency diverse flaw detection [1], parametric echo estimation [2], and joint time-frequency distribution [3]) on the RUSH platform using a Xilinx Virtex-5 FPGA with an embedded soft-core MicroBlaze processor [4,5] and a Xilinx Zynq 7020 FPGA with an embedded ARM processor [6,7] as shown in Figure 2.

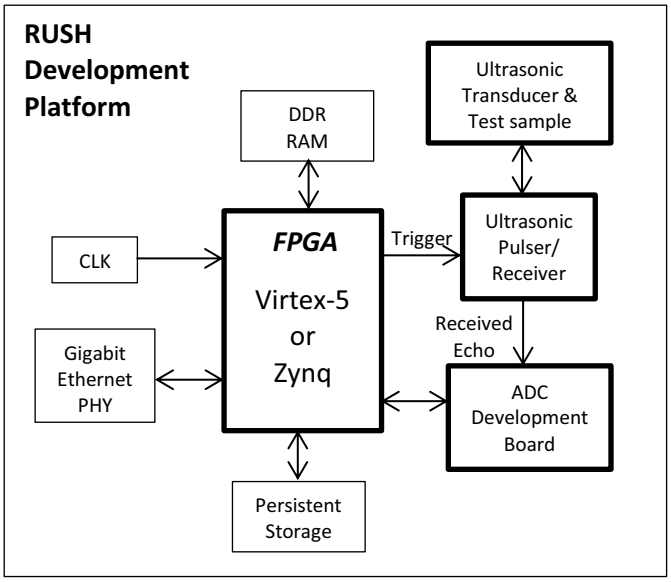

Figure 2. RUSH system block diagram

In ultrasonic nondestructive testing, the microstructures of the material cause the generation of scattering echoes which prevent the accurate detection of flaws. These scattering echoes can be reduced using split spectrum processing (SSP) [8,9]. SSP generates multiple subband signals by decomposing a broadband source, then recombining the signals using a post processing algorithm that reduces the energy of the scattering echoes. Our SSP algorithm uses basic one-zero windowing and an absolute minimum post processing block.

As ultrasonic signals are often composed of many interfering echoes and each echo can be modeled by a chirplet, the ultrasonic signal can be described using a set of six chirplet parameters per estimated echo by using the chirplet signal decomposition (CSD) [10,11] technique. Therefore, CSD results in a major data reduction (compression), and the compressed data can be used for data analysis and storage.

A chirplet signal can be defined as,

$$f_\theta(t) = \beta \exp[-\alpha_1(t-\tau)^2 + i2\pi f_c(t-\tau) + i\phi + i\alpha_2(t-\tau)^2] \quad (1)$$

This equation has six parameters $\Theta = [\tau, f_c, \beta, \alpha_2, \phi, \alpha_1]$ where term τ is the time-of-arrival, f_c is the center frequency, β is the amplitude, α_2 is the chirp rate, ϕ is the phase, and $\alpha_1$is the bandwidth factor of the echo. These parameter values are determined using the CSD algorithm such that they accurately model the echoes from the ultrasound experiments.

The execution performance of two types of time-frequency (t-f) distributions is examined - Wigner Ville distribution (WVD) and short time Fourier transform (STFT). Both WVD and STFT are powerful and highly practical techniques for analyzing dispersive signals in which different frequency contents arrive at different times. The WVD of an analog signal *f(t)* is given as

$$WVD_f(t,w) = \int_{-\infty}^{\infty} e^{-jw\tau} f\left(t+\frac{\tau}{2}\right) f^*\left(t-\frac{\tau}{2}\right) d\tau \quad (2)$$

The STFT of a signal is obtained by sliding a window and taking the Fourier transform of the windowed signal. In doing so it is assumed that the signal is stationary during the duration of the window [3]. STFT of a signal *s(t)* is obtained by calculating the spectrum of *s(τ)*. *h(τ-t)*, where *h(τ-t)* is the window function *h(t)* centered at t

$$STFT_s(t,w) = \int s(\tau)\, h(t-\tau) e^{-jw\tau} d\tau \quad (3)$$

and the spectrogram *SP(t,w)* is used for t-f analysis,

$$SP_s(t,w) = |STFT_s\,(t,w)|^2 \quad (4)$$

II. Embedded System Features

Two different FPGA based embedded systems (Xilinx Virtex-5 FPGA with embedded MicroBlaze processor and Xilinx Zynq all programmable system-on-chip with embedded ARM processor) are used in this study to analyze the performance of ultrasonic signal processing algorithms including SSP, CSD, WVD and STFT. The features of the embedded processors are summarized below.

The MicroBlaze is a soft-core processor optimized for the Xilinx FPGA fabric. Due to the soft-core nature of the processor, it can be configured to trade off performance or area utilization to optimize the processor for a given application. However, this configurability comes at a high cost to maximum performance, and this processor can only operate at a maximum frequency of 200 MHz. It can also be configured to run an operating system such as Linux to enhance the portability and reduce development time of applications. Furthermore, the performance of the MicroBlaze processor can be improved by configuring it to include peripherals such as floating point co-processor, integer divider, cache, direct memory access etc. [4,5].

The Zynq combines an ARM dual-core processing unit with a FPGA fabric. Unlike the MicroBlaze processor, the Zynq ARM processor is implemented in hardware and cannot be modified; however, it provides better performance. The Zynq provides a dual-core ARM Cortex-A9 processor based system at a maximum operating frequency of 1 GHz and 32 KB level-one (L1) instruction and data caches. Both Cortex-A9 processors execute the ARMv7-A instruction set and are equipped with a single instruction multiple data (SIMD) media processing engine (NEON). The NEON coprocessor's media and signal processing architecture adds instructions that target audio, video, image and speech processing and 3D graphics [6,7]. These advanced SIMD instructions help to execute the ultrasonic signal processing algorithms at a very high rate. The integration of some high-speed peripheral as hardware also provides a boost in performance while preserving the programmable logic for user applications.

Both Virtex-5 and Zynq integrate several components in their programmable logic arrays to accelerate digital signal processing operations such as FFT and digital filters. One example is the DSP48 blocks distributed around the FPGA to perform add-multiply-accumulate operations.

III. Performance Analysis of Ultrasonic Signal Processing Algorithms

This section presents the implementation and execution performance of ultrasonic signal processing algorithms namely SSP, CSD, WVD and STFT. For test tests, the MicroBlaze is maxed out with all possible floating point optimizations, a clock frequency of 100 MHz and 4 KB caches. The Zynq is running at the 533 MHz.

A. Split Spectrum Processing (SSP)

The execution time for SSP software implementation is estimated as follows. If *M* is the number of channels, SSP needs *M+1* FFT's. Given that one N-point FFT execution requires $2Nlog2(N)$ multiplications [13], where *N* is the total number of samples in the data, total execution time (in number of multiplications) becomes

$$T_{SSP} = 2(M+1)Nlog2(N) \quad (5)$$

From (5), it is clear that the execution time of SSP increases proportionally with the number of samples *N* and the number of channels *M.* The execution times for the SSP algorithm with 4, 8 and 12 channels on the Zynq ARM and Virtex-5 MicroBlaze processors are shown in Table I.

TABLE I. EXECUTION TIME OF SPLIT SPECTRUM PROCESSING ALGORITHM FOR A DATASET OF 2048 SAMPLES

Channels	Zynq ARM processor @ 533 MHz	Virtex-5 MicroBlaze processor @ 100 MHz
	Execution time (s)	**Execution time (s)**
4	0.1000	2.2323
8	0.1800	3.9761
12	0.2500	5.6057

Table I clearly shows that ARM processor performs 20 times faster than the MicroBlaze processor. Furthermore, it also can be interpreted that since the execution times are less than a second on the ARM, this algorithm implementation can run in real-time for many practical applications.

B. Chirplet Signal Decomposition (CSD)

CSD algorithm [7] has been optimized by using pre-computation and estimation methods. Additionally, the algorithm has been modified to provide stable and deterministic behavior for optimal parameter estimation. This implementation helps to reduce the execution time while maintaining an adequate accuracy for echo estimation. The algorithm performs several correlation operations to regenerate a chirplet with different parameters during each parameter estimation step. To reduce the execution time, correlation results are pre-computed and saved into a table for later use. Furthermore, by using coarse lookup tables for cosine, sine and tangent, the total execution time was substantially reduced with only a slight reduction in accuracy.

Execution times for the CSD algorithm on Virtex-5 MicroBlaze processor and Zynq ARM processor are listed in Table II. These results show a nearly linear increase in execution time with respect to number of echoes. As expected, it also shows that the SNR improves and exceeds 10 dB when 16 estimated echoes are combined. Furthermore, ARM processor outperforms the MicroBlaze processor by a factor of 150.

TABLE II. EXECUTION TIME AND SNR OF CHIRPLET SIGNAL DECOMPOSITION ALGORITHM FOR A DATASET OF 512 SAMPLES

Echoes	Zynq ARM processor @ 533 MHz		Virtex-5 MicroBlaze processor @ 100 MHz	
	Execution time (ms)	**SNR (dB)**	**Execution time (ms)**	**SNR (dB)**
1	10	1.06	820	1.06
2	10	2.46	1670	2.46
4	20	4.05	3240	4.05
8	40	6.73	6410	6.73
15	80	10.2	12160	10.2

C. Wigner-Ville Distributions (WVD)

From an implementation point of view, if we discretize the signal in both time and frequency, then the discrete Wigner-Ville distribution (WVD) of a finite discrete signal f(n) becomes [12].

$$WVD_{f(n.m)} = 2\sum_{k=-N+1}^{N+1} e^{-j\frac{km2\pi}{M}} f(n+k)f^*(n-k) \quad (6)$$

where *M = 2N - 1*. Note that the above equation is just a discrete Fourier transform (DFT) of the signal $f(n+k)f^*(n-k)$ for each time instant n. Hence fast Fourier transform (FFT) can be applied to reduce the calculation time [2].

If *N=2P* is the number of samples in the data, WVD requires

$$2[1+3+5+\cdots+(2P-1)] = 2(P)^2 = 2(N/2)^2 \quad (7)$$

complex multiplications. Each complex multiplication needs four regular multiplications. WVD also requires *N* number of N-point FFTs. Therefore, the total execution time (in number of multiplications) becomes

$$T_{WVD} = 8(\frac{N}{2})^2 + 2N^2 log2(N) \quad (8)$$

The execution time increases rapidly as N increases. The WVD execution times observed on Zynq ARM and Virtex-5 MicroBlaze processors are shown below.

TABLE III. EXECUTION TIME OF WIGNER-VILLE DISTRIBUTION ALGORITHM ON VARIOUS PROCESSORS

Number of samples in the signal	Zynq ARM processor @ 533 MHz	Virtex-5 MicroBlaze processor @ 100 MHz
	Execution time (ms)	**Execution time (ms)**
128	6.4	52.2
256	23.1	222
512	113.6	1948
1024	407.4	4573
2048	2015	21368

Table III indicates that the WVD can be executed in less than two seconds using ARM processor. However, MicroBlaze processor requires more time as the number of samples increases. This indicates that ARM processor is better suited for executing WVD in real time.

D. Short Time Fourier Transforms (STFT)

The performance of STFT depends on the window size chosen and the total number of time steps is required to obtain the t-f distribution. If *M* is the window size and *N* is the total number of samples in the signal, then *N-M* times M-point FFT's are required, which makes the total execution time (in number of multiplications) as

$$T_{STFT} = 2(N - M)Mlog2(M) \quad (9)$$

The window size M can be chosen by the user based on the specific application requirement. The above equation indicates that the execution time for STFT is proportional to square of the window size. The STFT execution times observed on Zynq ARM and Virtex-5 MicroBlaze embedded processors are shown below.

TABLE IV. EXECUTION TIME OF SHORT TIME FOURIER TRANSFORM ALGORITHM ON VARIOUS PROCESSORS FOR A DATASET OF 2048 SAMPLES AND A WINDOW SIZE OF 128 SAMPLES

Offset	Zynq ARM processor @ 533 MHz	Virtex-5 MicroBlaze processor @ 100 MHz
	Execution time (ms)	**Execution time (ms)**
1	84.5	1600
2	42.3	1300
4	21.2	150
8	10.2	84.0
16	5.3	33.5

From Table IV, and also by comparing (7) and (8), it is clear that STFT is much faster than WVD. However, WVD gives better resolution at the expense of cross terms.

IV. CONCLUSION

The SSP execution time for 2048 samples using the ARM processor embedded within the Zynq is only 0.1 second, whereas the same algorithm requires 2.2 seconds using the MicroBlaze processor within Virtex-5. Parametric echo estimation using chirplet signal decomposition (CSD) algorithm is also implemented on both the MicroBlaze and ARM embedded processors. The MicroBlaze processor takes one second to estimate one echo; while the ARM processor estimates 100 echoes per second. We also have examined time-frequency distributions including Wigner-Ville distribution and short-time Fourier transform for improved ultrasonic signal analysis and characterization. The computation time of WVD and STFT for 2048 data points is less than 2 seconds on the ARM processor. Our study proves that Zynq FPGA with an ARM processor computes the ultrasonic algorithms almost 30 times faster than the Virtex-5 FPGA with a MicroBlaze processor. The performance improvement of moving to newer and faster FPGAs undoubtedly demonstrates the advantages of using portable reconfigurable platforms for ultrasonic imaging and signal processing applications.

REFERENCES

[1] Y. Lu, E. Oruklu, J. Saniie, "Fast chirplet transform with FPGA-based implementation," *Signal Processing Letters, IEEE*, vol. 15, pp. 577–580, 2008.

[2] K.K. Chin, X.M. Jin, J. Saniie, "Spectral evaluation of ultrasonic flaw echoes using Wigner distribution", *IEEE Ultrasonics Symposium,* vol. 2, pp. 865-869, Dec 1990.

[3] M.A. Malik, J. Saniie, "Generalized time-frequency representation of ultrasonic signals", *IEEE Ultrasonics Symposium,* vol. 2, pp. 691-695, Nov 1990.

[4] V. Newhouse, N. Bilgutay, J. Saniie, E. Furgason, "Flaw-to-grain echo enhancement by split-spectrum processing," *Ultrasonics*, vol. 20, no. 2, pp. 59 – 68, 1982.

[5] Y. Lu, R. Demirli, G. Cardoso, and J. Saniie, "A successive parameter estimation algorithm for chirplet signal decomposition," *Ultrasonics, Ferroelectrics and Frequency Control, IEEE Transactions on*, vol. 53, no. 11, pp. 2121–2131, 2006.

[6] Xilinx, "Zynq-7000 All Programmable SoC Technical Reference Manual", UG585 (v1.5) March 7, 2013 [Online]. Available: http://www.xilinx.com/support/documentation/user_guides/ug585-Zynq-7000-TRM.pdf

[7] J. Saniie, E. Oruklu, S. Yoon, "System-on-chip design for ultrasonic target detection using split-spectrum processing and neural networks," *IEEE Transactions on Ultrasonics, Ferroelectrics and Frequency Control,* vol. 59, no. 7, pp. 1354–1368, 2012.

[8] J. Saniie, T. Wang, X. Jin, "Frequency diverse Bayesian ultrasonic flaw detection," *IEEE Ultrasonics Symposium,* vol. 2, pp. 1135-1138, Oct 1989.

[9] R. Demirli, J. Saniie, Model-based estimation of ultrasonic echoes, Part II: Nondestructive evaluation applications", *IEEE Transactions on Ultrasonics, Ferroelectrics and Frequency Control,* vol. 48, no. 3, pp. 803-811, 2002.

[10] Xilinx, "Virtex-5 FPGA Data Sheet," 2012. [Online]. Available: http://www.xilinx.com/

[11] Xilinx, "Zynq-7000 All Programmable SoC Overview", DS190 (v1.3) March 15, 2013 [Online]. Available: http://www.xilinx.com/support/documentation/data_sheets/ds190-Zynq-7000-Overview.pdf

[12] Xilinx, "Virtex-5 FPGA user guide," UG190 (v5.4) March 16, 2012. [Online].Available: http://www.xilinx.com/support/documentation/user_guides/ug190.pdf

[13] J.G Proakis, D.G. Manolakis, "Efficient Computation of the DFT: Fast Fourier Transform Algorithms", in Digital Signal Processing: Principles, Algorithms and Applications, 4th ed., *Pearson*, 2011.