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Hardware-Software Co-design of 3D Data Compression for Real-time Ultrasonic Imaging Applications

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***Abstract* - Many of the ultrasonic NDE and imaging applications require processing of huge amount of data in real-time. Compression of acquired data helps to reduce the storage and to rapidly transmit information to remote locations for further analysis. Signal fidelity, computational speed and resource utilization are the major parameters to be considered while designing the architecture for the compression algorithm. The objective of this study is to implement discrete wavelet transform (DWT) based ultrasonic 3D data compression algorithm on a reconfigurable ultrasonic system-on-chip hardware platform targeted for real-time ultrasonic imaging applications. The reconfigurable platform allows analysis of multiple architectures to suit various applications. The algorithm is implemented as a hardware-only design and hardware-software co-design. Both implementations provide a high signal compression ratio of about 98% with good quality signal reconstruction. This study demonstrates that, compressing 33 MBytes of experimental ultrasonic 3D data into 0.4 MBytes requires only one-fourth of a second for hardware-only design, and one minute for hardware-software co-design, making both designs highly suitable for real-time ultrasonic imaging applications.**

I. Introduction

During the last few years, there is an increased focus on using ultrasound imaging for medical applications due to the non-ionizing diagnostic capability of ultrasound, unlike the other classical diagnostic methods such as X-rays, computed tomography etc. which causes harmful effects to the human body. As the technology advances to develop portable and hand-held ultrasound units, more medical and industrial applications are expected to use ultrasound imaging techniques in the future. These applications require huge amount of data processing as part of the diagnostic analysis. Likewise, the point of care technology and remote health monitoring which are being implemented in current days, demands high volumes of information to be transmitted via internet to remote locations for expert analysis. This demands compressing the data without losing the required information. Furthermore, the computation time for the compression is critical for real-time applications, where faster diagnosis is essential due to the severity of the health condition.

The modern embedded hardware systems along with the latest software applications can provide an improved platform to execute ultrasonic imaging applications in a highly efficient manner. Furthermore, reconfigurable hardware platforms based on field-programmable gate arrays (FPGAs) are highly suitable for applications which demand lower cost and high flexibility [1] [2]. The embedded processing platforms consist of highly integrated system-on-chips (SoC) which combine powerful processors such as ARM with programmable hardware units for high speed signal processing.

In this study, the ultrasonic 3D data compression algorithm is implemented on a Xilinx Zynq-7020 all programmable SoC platform which integrates an efficient dual-core ARM Cortex™-A9 MPCore™-based processing system along with Xilinx FPGA programmable logic in a single device [3]. Additionally, the implementation on Zynq dual core ARM processor is compared against a software implementation on a low cost single core ARM processor available on Raspberry Pi platform [4].

The processor-centric approach of the Zynq platform permits the ARM processor to hold the overall control of the embedded system. Furthermore, partial reconfiguration of the programmable logic is also controlled by the ARM processor. Thus the user is able to optimize the system performance to meet the various application requirements.

II. Ultrasonic 3D Data Compression

Many medical diagnostic and industrial applications require processing of massive amount of volumetric information. This demands acquisition of ultrasonic data by using 3D scanning of the tissue or material as shown in Figure 1. In this study, a 3D block of data consisting of several interfering echoes is acquired using a 5 MHz ultrasonic broadband transducer and a steel block specimen with microstructural defects.

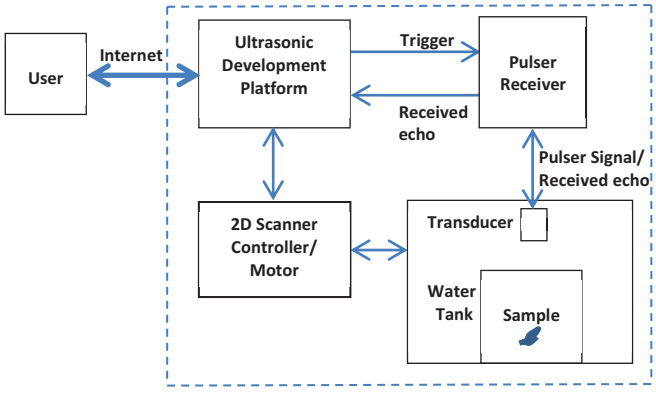

Figure 1. Ultrasound testing setup

The model of this volumetric data of 2048x128x128 bytes (33 MBytes) is shown in Figure 2a. To reduce the amount of data to be transferred, 3D data compression is performed by the ultrasonic development platform (see Figure 1) using successive 1D compressions on x, y and z directions [5] [6], as shown in Figure 2b.

In this study, discrete wavelet transform (DWT) is used for compressing ultrasonic data. The high energy compaction property of DWT is utilized here to achieve maximum compression without sacrificing the quality of signal reconstruction. DWT is based on multistage sub-band decomposition [7] which is carefully structured to isolate high energy sub-bands to provide maximum signal compression with high signal fidelity. After several experimentations with different wavelet basis, it has been determined that daubechies-10 (Db10) wavelet gives the best compression of ultrasonic experimental data with minimal reconstruction error in the x-direction. As shown in Figure 3, a four level decomposition structure is designed to isolate the high energy frequency sub-bands in order to achieve maximum compression in x-direction. A simple Haar wavelet is used for decomposition in the y and z directions to maintain high computational performance. Our experimentations show that, after the decomposition in x-direction, the sub-bands H, LH and LLHL carry very low energy, and thus can be eliminated. The remaining sub-bands LLL (256 samples) and LLHH (128 samples) constitute only 20% of the total signal samples. This indicates 80% compression in x-direction. An additional 75% compression is achieved in y-direction and a further 75% compression in z-direction. Thus the overall 3D compression becomes 98.7%.

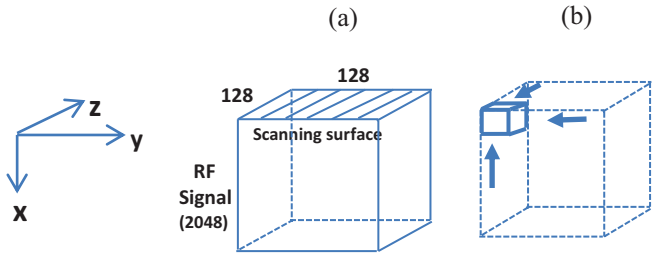

Figure 2. (a) 3D ultrasonic data block, and (b) 3D compressed data.

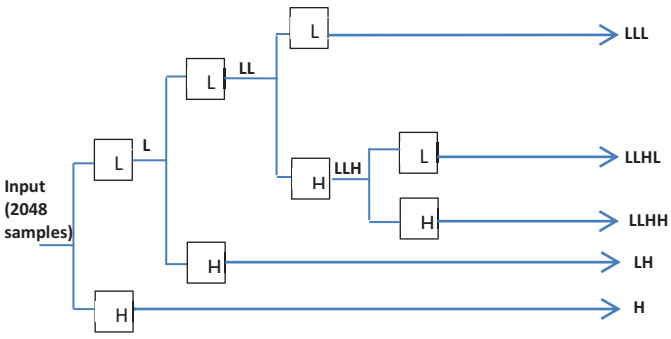

Figure 3. Wavelet packet decomposition in x-direction

III. Implementation of 3D Data Compression on Zynq Platform

The ultrasonic compression algorithm using 3D DWT is implemented on a Xilinx Zynq-7020 all programmable system-on-chip FPGA which embeds an ARM processor unit. The ARM processor unit contains two ARM Cortex A9 processor cores with NEON co-processors that are connected in multi-processor configuration. This greatly benefits the efficient hardware-software (HW/SW) co-design of 3D ultrasonic data compression. As shown in Figure 4, in the Zynq SoC, the programmable logic is tightly integrated with the ARM processor unit via high speed AXI interface. Furthermore, the direct memory access (DMA) capability enables faster data transfers between the processor and external DDR memory. This allows flexibility to develop the system by efficiently partitioning the hardware and software modules according to the application requirement.

Two implementation methods of the compression algorithm are discussed in this study: (i) hardware-only design using programmable logic, and (ii) HW/SW co-design using ARM processor and programmable logic. DWT mainly requires filtering operations, which involves several multiplications. In this study, filtering is performed by convolving the signal samples with the Db10 filter coefficients for x-direction, and Haar coefficients for y and z directions. Additionally, for the hardware-only design, the lowpass and highpass filters are processed in parallel to further reduce the overall execution time. In the HW/SW co-design approach, the Zynq platform is used to implement the compression algorithm in real-time, wherein the ultrasonic data acquisition via ADC is controlled in programmable logic hardware, and the compression algorithm is executed in software by the ARM processor (see Figure 4).

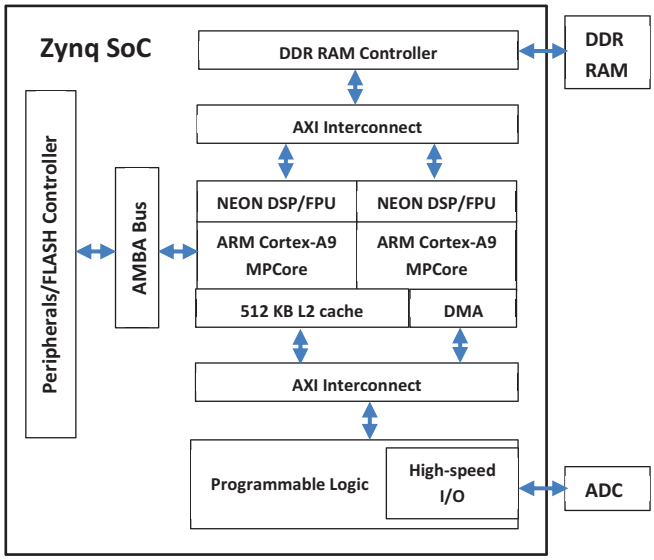

Figure 4. Zynq 7020 architecture block diagram

A. Hardware-only Design

In the hardware-only design, polyphase filters [8] are used instead of conventional filters for the first 2 stages of decomposition, to improve the computational efficiency and hardware resource utilization. As shown in Figure 5, the polyphase architecture operates simultaneously on the even samples [X(2k)] and the odd samples [X(2k+1)] of the input. Thus the filtering operation requires only half the time compared to conventional filters. Furthermore, since the filtered output needs to be sub-sampled, we can eliminate either the even or odd sample output. In this study, we have eliminated the odd samples [Y(2k+1)]. As shown in Figure 5, the H_{odd} filter applied to the even inputs, and the H_{even} filter applied to the odd inputs (shown in 'red' color) are not required. Thus the filtering operation requires only half the resources compared to conventional filters. The polyphase filters are not accurate for the last 2 stages of decomposition, since the sampling frequency is very low in these stages. Therefore, conventional filters are used for the last 2 stages of decomposition. Since the number of samples in the last 2 stages is relatively low, the use of conventional filters will not significantly affect the computational efficiency and resource utilization.

During signal reconstruction, the compressed data is interpolated before filtering operation is performed. Thus, the odd samples [X(2k+1)] will always be zero. Therefore, only the upper section (one set of even and odd filters) of the polyphase architecture is needed, which further reduces the hardware resource utilization.

B. Hardware/Software Co-design

The block diagram shown in Figure 6 describes the HW/SW co-design architecture for capturing the ultrasonic signal and performing signal compression in real-time. The data capture hardware block within Zynq SoC collects data from ultrasonic scanning system and stores into DDR memory. ARM processor reads this 3D volumetric data from DDR memory and executes the compression algorithm in software. The compressed data is then stored back to the DDR memory, which can be transferred to remote locations for expert analysis.

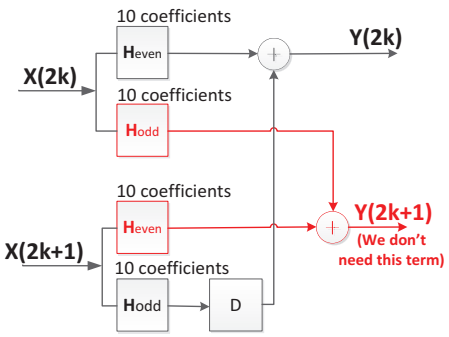

Figure 5. Polyphase filter used for decomposition

The software implementation of the 3D compression algorithm utilizes multi-processor capability of ARM processor unit within Zynq, to improve the computational performance. In this study, the parallel processing capabilities of OpenMP [9] is utilized to improve the performance of the compression algorithm execution in software. OpenMP uses specific compiler directives and flags to produce an output which is compatible for multicore processing. The compression and reconstruction processes are optimized by using two threads per each ARM core. This helps to distribute the work load and to complete the compression/reconstruction operations rapidly.

The decomposition process involves filtering and sub-sampling. One A-scan consisting of 2048 samples is read from the memory at a time, which is sub-sampled and filtered using Db10 wavelet coefficients at each of the four stages (see Figure 3) to achieve maximum compression in x-direction. This process is repeated for all the A-scans (128x128 = 16384 A-scans). The filtering process is performed on the sub-sampled signal to improve the execution speed by a factor of 2. In the y and z directions, the filtering is performed with Haar wavelet coefficients. Furthermore, only two-stage decomposition is required for maximum compression in y and z directions. After the 3D compression, the resultant data is reduced to 32x32x384 bytes (0.4 MBytes) from the original size of 2048x128x128 bytes (33 MBytes).

Reconstruction is a similar and reverse process of compression. Initially, the processing is performed in z-direction, followed by processing in y-direction, and finally in x-direction to retrieve the complete 3D ultrasonic data.

IV. Performance Analysis

In this section, the quality of compression/reconstruction, and the computational performance are analyzed for both hardware-only design and HW/SW co-design of ultrasonic 3D data compression.

The quality of compression and reconstruction is analyzed by calculating the correlation between the original signal and the 3D reconstructed signal. The correlation analysis for

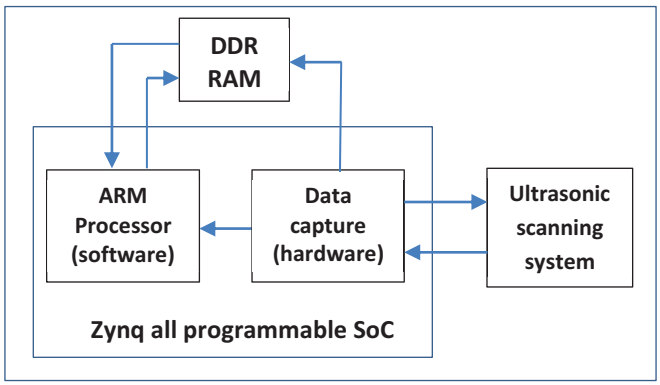

Figure 6 HW/SW co-design architecture for 3D ultrasonic signal compression

the hardware-only design provides 81% similarity between original and 3D reconstructed data, whereas the HW/SW co-design provides a similarity of 80%.

A. Computational Performance of Hardware-only Design

Table I shows the computational performance for hardware-only design of ultrasonic 3D compression implemented on Zynq programmable logic running at a clock rate of 200 MHz. In this implementation, the overall 3D compression (compressing a volumetric data of 33 MBytes into 0.4 MBytes), is completed in one-fourth of a second, which indicates a very high speed compression suitable for rapid transmission of data to remote locations via Internet.

Table I. Computational performance for hardware-only design of ultrasonic 3D compression implemented on Zynq programmable logic running at 200 MHz.

	Computational Time (seconds)
X - compression	0.19
Y - compression	0.05
Z - compression	0.01
Overall 3D compression	**0.25**

B. Computational Performance of HW/SW Co-design

The computational performance for HW/SW co-design of the ultrasonic 3D compression algorithm is described in Table II with a comparison against a software implementation on single core ARM processor available on Raspberry Pi platform.

From Table II, it can be seen that Zynq dual core ARM performs close to twice faster compared to the single core ARM on Raspberry Pi. Furthermore, the HW/SW co-design on Zynq SoC requires only one minute for compressing 33 MBytes of ultrasonic data into 0.4 Mbytes, which indicates that this implementation is highly suitable for real-time ultrasonic imaging applications.

Table II. Computational performance for HW/SW co-design of ultrasonic 3D compression.

	Zynq ARM Dual Core at 666 MHz (seconds)	Raspberry Pi ARM Single Core at 700 MHz (seconds)
X - compression	64	99.29
Y - compression	1.1	1.9
Z - compression	0.25	0.73
Overall 3D compression	**65.35**	**101.92**

V. CONCLUSION

Ultrasonic medical and NDE imaging applications require large amount of data to be transmitted to distant locations for expert analysis. Compressing huge volumetric data is essential for ensuring rapid data transmission. Reconfigurable platforms can be used to efficiently compress the data within a short time, which is critical for real-time ultrasonic imaging applications. This study demonstrates two efficient implementations (hardware-only design and HW/SW co-design) of ultrasonic 3D data compression algorithms on Xilinx Zynq-7020 all programmable system-on-chip platform which embeds an ARM processor unit. Hardware-only design compresses the volumetric image of 33 MBytes into 0.4 MBytes in 0.25 seconds, whereas the HW/SW co-design completes the compression in one minute, making both designs highly suitable for real-time ultrasonic imaging applications. Furthermore, both implementations provide a compression ratio of 98% with high quality signal reconstruction.

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