

Floating Point Hardware and Software Realization for Adaptive FIR Fetal ECG Estimation

Sizhou Wang and Jafar Saniie

*Department of Electrical and Computer Engineering
Illinois Institute of Technology, Chicago, Illinois, USA*

Abstract — This paper presents realizations of IEEE-754 single precision floating point non-invasive fetal ECG estimation based on QR Decomposition Recursive Least Square algorithm (QRD-RLS). Experiments of the system, which is implemented on Xilinx Zynq SoC platform, are carried out with electrocardiogram (ECG) data and the results with analysis are presented. The embedded system design aims for hardware optimization by saving arithmetic resources, streaming pipeline performance and software-aid computation and integration. The challenge of exploiting the system full potential with pseudo-parallel computation on multiple fetal ECG data packets is also examined.

I. INTRODUCTION AND BACKGROUND

Since early 20th century, there have been various studies on fetal monitoring and obtaining information about the fetal heart status with electrocardiography (ECG), which is to represent electrical activity of heart plotted on paper. Non-invasive electrocardiography exposes itself as a very useful method to obtain reliable information about the child's health condition during pregnancy. In practice, it is impossible to isolate fetal ECG through traditional frequency selective filtering [1]. Furthermore, the procedure of extracting fetal ECG usually requires high levels of accuracy in its calculations and presentations.

Adaptive FIR filtering is considered important for unknown system identification, noise cancellation and bio-signal extraction [2]. This method performs well for estimating the fetal ECG from the maternal abdomen [3]. However, adaptive filtering is computationally heavy and real-time implementation becomes very difficult. Therefore, to overcome the existing difficulty, the QR Decomposition (QRD) based Recursive Least Square (RLS) algorithm [4] is adopted. To solve the RLS problem, Givens Rotation can be implemented as streaming pipeline hardware which is a triangular systolic array proposed by Gentleman and Kung [5]. This approach turns out to be resource effective even when the whole computation procedure is in IEEE-754 floating point [6].

The overall adaptive filter structure is shown in Figure 1. To satisfy the requirements of accurate calculation, single precision floating point operation is implemented. The

adaptive algorithm used in this system is illustrated in Section II. In Section III, we describe our elaborations on verifying the accuracy of the system and the estimated fetal ECG signal based on 2-channel recordings of a pregnant woman provided by DaISy database [7]. We will also introduce time-division methodology to increase the system throughput by implementing pseudo-parallelism, which is to process multiple ECG estimations concurrently.

II. REALIZATION AND METHOD

A. System Overview

The major component of the hardware system is Xilinx Zynq SoC FPGA [8]. This enables hardware-software co-design for optimized system performance. Our system design concentrates on the computation accuracy and provides real-time signal processing for non-invasive fetal ECG extraction and unknown FIR system identification.

The system (see Figure 2) can be sub-divided into two parts: the hardware-oriented floating point QRD-RLS pipeline core, and software-oriented ARM-NEON general operation core. The floating point QRD-RLS core operates at maximum frequency of 28 MHz in real-time.

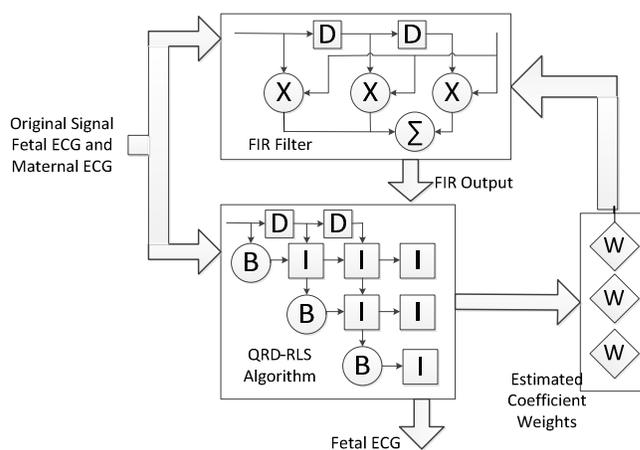


Figure 1. Adaptive FIR structure adopted to perform fetal ECG estimation. (B: boundary cell, I: internal cell, W: coefficient weight computation.)

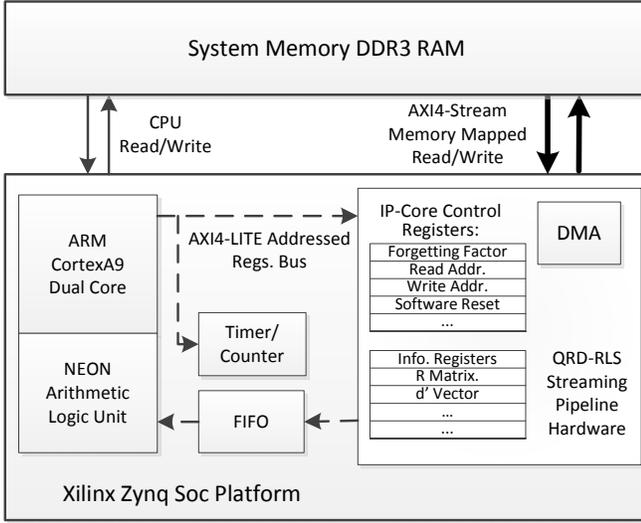


Figure 2. System realization architecture

The VHDL code for FPGA implementation is optimized by deep pipelining. For this implementation, the streaming latency for each operation is 30 clock cycles. A Direct Memory Access (DMA) unit is specially designed for pipeline operation which directly reads and writes to the system memory, and thus releases the CPU during the computation by the hardware. By this arrangement, the CPU can be assigned to other processes, such as preparing for the next operation, receiving/sending samples or telecommunication with other platform. The FPGA resource usage for adaptive fetal ECG estimation is summarized in Table I. Additionally, the power consumption of the system is roughly 1.139W estimated by the Xilinx power estimator tool.

TABLE I. SYNTHESIS RESULTS

Slices:	92%:	12289/13300
LUTs:	75%:	39949/53200
RAMB36E1:	3%:	74/140
DSP48E1:	45%:	99/220
Registers:	6%:	7168/106400

B. Algorithm for fetal ECG estimation

Adaptive FIR filter based on QRD-RLS algorithm is designed to perform fetal ECG estimation (See Figure 1). This adaptive algorithm is used to solve the least square problem by minimizing the sum of n square errors as shown in (1):

$$\min(\lambda_{n \times n} \mathbf{e}_{n \times 1}^2) = \min(\mathbf{e}_{n \times 1}^T \lambda_{n \times n} \mathbf{e}_{n \times 1}) \quad (1)$$

where $\lambda_{n \times n}$ is the forgetting factor diagonal matrix (with element λ_0 less than 1) which can be adjusted to weigh more on the most recent samples. Element λ_n can be expressed as:

$$\lambda_n = (\lambda_0)^n, \quad (0 \leq n < \infty) \quad (2)$$

The error vector $\mathbf{e}_{n \times 1}$ with size n in the adaptive FIR filtering is defined as the difference between FIR input and FIR output (see Figure 1), which in this case correspond to mixed

mother/child ECG signal (FIR input) and mother ECG signal (FIR output). As a result, the error is the fetal ECG signal that we intend to estimate. This relation is defined in Equation (3).

$$\mathbf{e}_{n \times 1} = \mathbf{X}_{n \times k} \mathbf{w}_{k \times 1} - \mathbf{d}_{n \times 1} \quad (3)$$

where vector $\mathbf{w}_{k \times 1}$ refers to the FIR filter coefficient (k represents the number of FIR coefficients); matrix $\mathbf{X}_{n \times k}$ is the input correlation matrix formed from the FIR input signal, see Equation (4); vector $\mathbf{d}_{n \times 1}$ stands for desired FIR output signal.

$$\mathbf{X}_{n \times k} = \begin{bmatrix} x_{n-1} & x_{n-2} & \dots & x_{n-k+1} & x_{n-k} \\ x_{n-2} & x_{n-3} & \dots & x_{n-k} & x_{n-k-1} \\ x_{n-3} & x_{n-4} & \dots & x_{n-k-1} & x_{n-k-2} \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ x_{k-2} & x_{k-1} & \dots & x_2 & x_1 \\ x_{k-1} & x_{k-2} & \dots & x_1 & x_0 \\ \vdots & \vdots & \dots & \vdots & \vdots \\ x_1 & x_0 & \dots & 0 & 0 \\ x_0 & 0 & \dots & 0 & 0 \end{bmatrix} \quad (4)$$

We define matrix $\mathbf{D}_{k \times k, i}$ as a sub-matrix of $\mathbf{X}_{n \times k}$ with row (k-1+i) to row i of matrix $\mathbf{X}_{n \times k}$,

$$\mathbf{D}_{k \times k, i} = \begin{bmatrix} x_{k+i-1} & x_{k+i-2} & \dots & x_i \\ x_{k+i-2} & x_{k+i-3} & \dots & x_{i-1} \\ \vdots & \vdots & \ddots & \vdots \\ x_i & x_{i-1} & \dots & x_{i-k+1} \end{bmatrix} \quad (5)$$

The matrix $\mathbf{D}_{k \times k, i}$ can be further transformed to a product of an orthogonal matrix $\mathbf{Q}_{k \times k, i}$ and an upper triangular matrix $\mathbf{R}_{k \times k, i}$ by QR decomposition:

$$\mathbf{Q}_{k \times k, i} \times \mathbf{R}_{k \times k, i} = \mathbf{D}_{k \times k, i} \quad (6)$$

$\mathbf{X}_{n \times k}$ is updated by replacing its sub-matrix $\mathbf{D}_{k \times k, i}$ by matrix $\mathbf{R}_{k \times k, i}$, and then $\mathbf{X}_{n \times k}$ is further updated by $\mathbf{D}_{k \times k, i+1}$ and $\mathbf{R}_{k \times k, i+1}$. After n series of such updates from i=0 to i=n-1, $\mathbf{X}_{n \times k}$ can be transformed into an upper triangular matrix as shown in Equation (7). This relation then can be expressed in Equation (8).

$$\mathbf{R}_{n \times k} = \begin{bmatrix} r_{0,0} & r_{0,1} & r_{0,2} & \dots & r_{0,k-1} \\ 0 & r_{1,1} & r_{1,2} & \dots & r_{1,k-1} \\ 0 & 0 & r_{2,2} & \dots & r_{2,k-1} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & \dots & r_{k-1,k-1} \\ 0 & 0 & 0 & \dots & 0 \\ \vdots & \vdots & \vdots & \dots & \vdots \end{bmatrix} \quad (7)$$

$$\prod_{i=0}^n \{\mathbf{Q}_{k \times k, i}\} \boxtimes \mathbf{R}_{n \times k} = \mathbf{X}_{n \times k} \quad (8)$$

Such a series of operation is based on Givens rotation [9], and denoted by operator \boxtimes , which is realized in systolic array shown in Figure 1. Since $\mathbf{Q}_{k \times k, i}$ is orthogonal matrix, the product of this matrix with its transpose is an identity matrix:

$$\mathbf{Q}_{k \times k, i} \times \mathbf{Q}_{k \times k, i}^T = \mathbf{I}_{k \times k, i} \quad (9)$$

If we carry out this series of operation by applying n matrices of $\mathbf{Q}_{k \times k, i}$ to vector $\mathbf{e}_{n \times 1}$, we can rewrite Equation (1) by assuming λ as an identity matrix:

$$\begin{aligned} \min(\mathbf{e}_{n \times 1}^T \mathbf{e}_{n \times 1}) &= \min(\mathbf{e}_{n \times 1}^T \mathbf{Q}_{k \times k, i} \mathbf{Q}_{k \times k, i}^T \mathbf{e}_{n \times 1}) \\ &= \min((\mathbf{Q}_{k \times k, i}^T \mathbf{e}_{n \times 1})^T \mathbf{Q}_{k \times k, i}^T \mathbf{e}_{n \times 1}) \\ &= \min((\mathbf{Q}_{k \times k, i}^T \mathbf{e}_{n \times 1})^2) \end{aligned} \quad (10)$$

Besides, substituting (9) to (8) we have:

$$\mathbf{R}_{n \times k} = \sum_{i=0}^n \{\mathbf{Q}_{k \times k, i}^T\} \boxtimes \mathbf{X}_{n \times k} \quad (11)$$

Equation (11) also indicates solving least square problem by applying the operation with n matrices of $\mathbf{Q}_{k \times k, i}^T$ to both sides of Equation (3),

$$\sum_{i=0}^n \{\mathbf{Q}_{k \times k, i}^T\} \boxtimes \mathbf{e}_{n \times 1} = \mathbf{R}_{n \times k} \mathbf{w}_{k \times 1} - \mathbf{d}'_{n \times 1} \quad (12)$$

where,

$$\mathbf{d}'_{n \times 1} = \sum_{i=0}^n \{\mathbf{Q}_{k \times k, i}^T\} \boxtimes \mathbf{d}_{n \times 1} \quad (13)$$

If we split $\mathbf{d}'_{n \times 1}$ into vector $\mathbf{u}_{k \times 1}$ of size k and $\mathbf{a}_{(n-k) \times 1}$ of size $n-k$, then we can rewrite Equation (12) as Equation (14):

$$\sum_{i=0}^n \{\mathbf{Q}_{k \times k, i}^T\} \boxtimes \mathbf{e}_{n \times 1} = \begin{vmatrix} \mathbf{R}_{k \times k} \times \mathbf{w}_{k \times 1} \\ 0 \end{vmatrix} - \begin{vmatrix} \mathbf{u}_{k \times 1} \\ \mathbf{a}_{(n-k) \times 1} \end{vmatrix} \quad (14)$$

With Equation (14), it is noticeable that the problem of minimizing Equation (1) would be,

$$\min((\mathbf{R}_{k \times k} \times \mathbf{w}_{k \times 1} - \mathbf{u}_{k \times 1})^2) \quad (15)$$

Finally, if we define vector $\mathbf{u}_{k \times 1}$ is the minimum value of above expression, minimized error vector \mathbf{e}_n , or the estimated fetal ECG signal would be:

$$\mathbf{e}_{n \times 1} = \begin{vmatrix} \mathbf{u}_{k \times 1} \\ \mathbf{a}_{(n-k) \times 1} \end{vmatrix} \quad (16)$$

$\mathbf{a}_{(n-k) \times 1}$ is actually the output of the bottom internal cell (I) on the right column (see Figure 1). The above derivation did not include the forgetting factor, which only scales the $\mathbf{e}_{n \times 1}$ vector. It is implicitly applied to QR decomposition and updated R matrix [10].

C. Hardware and Software Implementation Considerations.

QR Decomposition and back substitution for filter coefficient is optimized for hardware implementation. Normally boundary cell (shown in Figure 1) performs [9]:

$$S_n = \frac{\sqrt{\lambda} r_n}{\sqrt{\lambda R_n^2 + x_n^2}}, \quad C_n = \frac{x_n}{\sqrt{\lambda R_n^2 + x_n^2}}, \quad R_n = \sqrt{\lambda R_{n-1}^2 + x_n^2} \quad (17)$$

If we replace the division and square root with reciprocal square root, the most recent r value is calculated by the input and output of the reciprocal square root operation. Furthermore, the updated R value in this cell is consequently transformed to $1/R$, which is essentially helpful for the subsequent back-substitution operations. Figure 3 presents timing Data Flow Graph (DFG) for Boundary Cell (B). The flip-flop in cycle 5 stores R_n when the one in cycle 2 stores R_{n-3} .

Through this method, the hardware resource consumption of back substitution is reduced up to 40%, especially for lower depth filter structures.

Generally, the software performs multiple operations, such as preparing data, configuring hardware control registers, and

responding to hardware interrupt. The procedures are described more precisely in software/hardware flow chart in Figure 4.

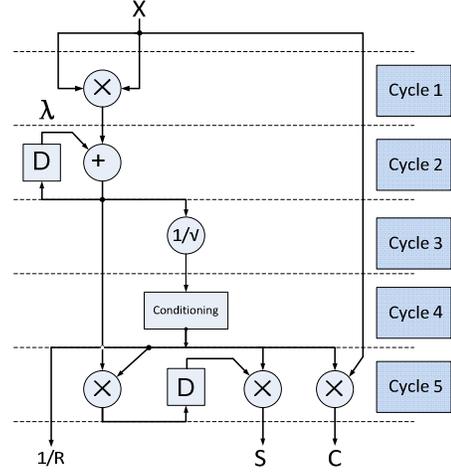


Figure 3. Timing Data Flow Graph (DFG) for Boundary Cell

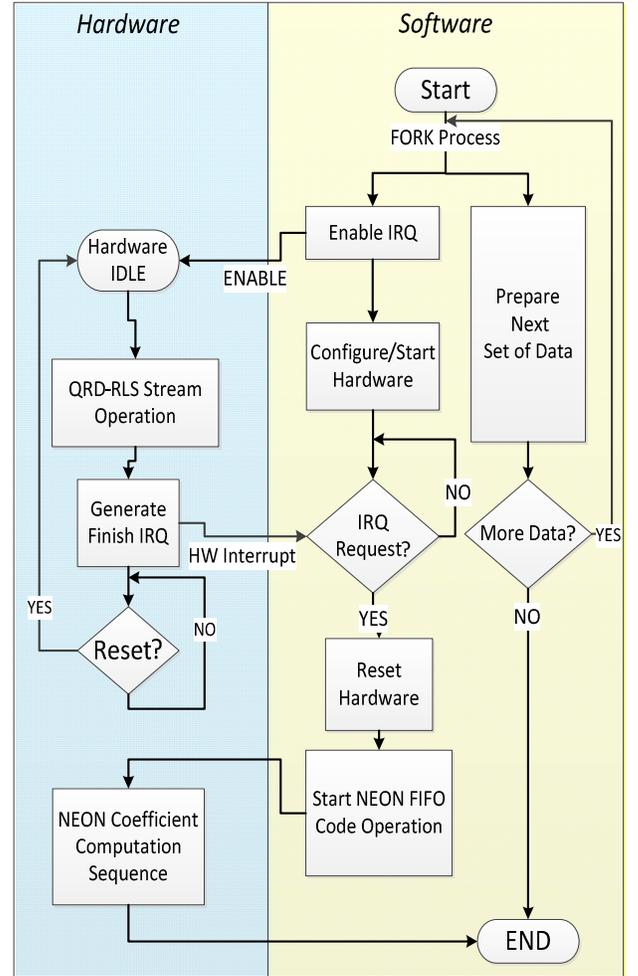


Figure 4. Software/hardware control flowchart

To better understand the overall capability of the system, a timing stamp based on 2500 samples per packet (a packet implies one ECG signal segment) is shown in Figure 5. The timer/counter (see Figure 2) is responsible for recording the actual operation and procedure timings.

The fetal ECG estimation time depends on number of samples in a packet, and the cross-platform data acquisition time for each packet. If we consider each ECG packet consists of 2500 samples, based on the data we have obtained with processing of ECG samples on Zynq platform, at least 5000 ECG packets can be processed in one second.

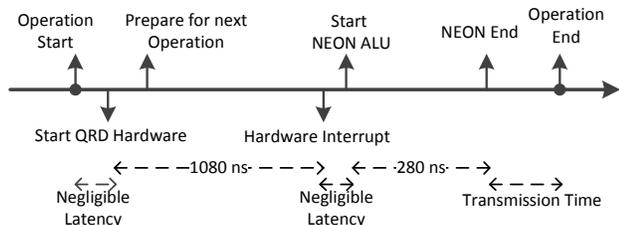


Figure 5. Time stamp in processing one ECG packet (Negligible Latency is negligible amount of CPU time; Transmission Time depends on data exchange conditions.)

III. VERIFICATION AND RESULT

A. FIR System Identification

Consider the 3-stage FIR system described in Equation (18), where $x(n)$ is the n^{th} input and $y(n)$ is the output:

$$y(n) = 0.1258x(n) + 0.2515x(n-1) + 0.1258x(n) \quad (18)$$

We assumed the above FIR system is unknown. We used the developed hardware/software adaptive algorithm to estimate the FIR coefficients with a set of random input signals. As we process more data points, the estimated FIR coefficients become more accurate (exact values were estimated within 7 decimal-point accuracy). The estimation took less than 120 samples or 4.325 microseconds processing time to train the adaptive filter into a stable state.

B. Fetal ECG Estimation

The fetal ECG extraction result is based on cutaneous potential recordings of a pregnant woman provided by DaISy database [7]. For this study, two ECG signal (maternal abdominal ECG and maternal thoracic ECG) are selected to estimate the fetal ECG. The sampling rate of the maternal ECG is 250 Hz, and the number of samples is 1200, which is equivalent to about 5 seconds of recording.

The maternal abdomen signal contains both maternal and fetus ECG on the first row of Figure 6. The following row shows maternal thoracic signal which only contains maternal ECG. The bottom row is the estimated fetal ECG signal using both software and hardware for estimation. It can be seen that the extracted fetal heart beat rate is higher than the maternal heart beat rate.

IV. CONCLUSION

In this study, an Adaptive FIR system is developed to perform fetal ECG estimation. The system is verified with coefficient weight estimation. The floating point QRD-RLS algorithm used in our system demonstrates high accuracy and resource effectiveness. The fetal ECG estimation result proves satisfactory estimation performance of the algorithm.

Our future work is focused on further analyzing estimated fetal ECG models, tackling problems on clinical data experiments and extending the parallelism of our system.

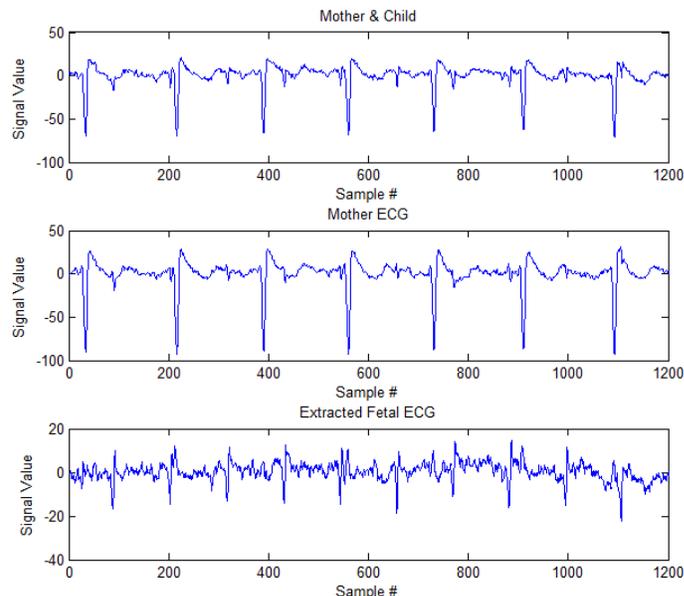


Figure 6. Fetal ECG estimation (lower trace) of 1200 samples. Top trace is mother and fetal mixed ECG signal. Middle trace is mother ECG signal.

REFERENCES

- [1] B. Widrow; *Adaptive Signal Processing*, Prentice Hall, 1985.
- [2] G. Camps ; M. Martinez ; E. Soria ; , "Fetal ECG Extraction using an FIR Neural Network," University of Valencia, Spain, 2001.
- [3] Fetal ECG extraction; , National Instruments[online]. Available: <http://www.ni.com/white-paper/11248/en/>
- [4] S. Niu; W. Sizhou; J. Saniie; , "Hardware and Software Design for QR Decomposition Recursive Least Square Algorithm," *IEEE 56th IMSCS*, 8321, Aug. 5-8, 2013.
- [5] W.M. Gentleman; H.T. Kung; , "Matrix Triangularization by Systolic Arrays," in *Proceedings of SPIE- The International Society for Optical Engineering*, vol. 298, Aug. 25-28, 1981.
- [6] M.D.Ercegovic; T.Lang; , *Digital Arithmetic*, Morgan Kaufmann Publishers, 2004.
- [7] DaISy [Online]. Available : <http://homes.esat.kuleuven.be/~smc/daisy/>
- [8] Xilinx. Zynq. Zedboard[Online]. Available: <http://www.xilinx.com>
- [9] S. Aslan; S. Niu; J. Saniie; , "FPGA Implementation of Fast QR Decomposition Based on Givens Rotation," *IEEE 55th IMSCS*, pp.470-473, Aug. 5-8, 2012.
- [10] Proudler, I.K; McWhirter, J.G; , "Computationally efficient QR decomposition approach to least squares adaptive filtering" *Radar and Signal Processing, IEE Proceedings F*, Aug. 1991.