Programmable Analog Front-End System for Ultrasonic SoC Hardware

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***Abstract* – This study presents a scheme for enhancing the capabilities of an ultrasonic hardware platform leading to a fully reconfigurable system allowing for dynamic control over the analog front-end. This system presents a robust approach for nondestructive testing, data analysis and imaging applications. The fully programmable analog front-end system proposed in this paper supports up to 8 ultrasonic sensors. The components of this system are dynamically configurable by a Zynq system-on-chip (SoC) module for real-time ultrasonic data acquisition and analysis. This reconfigurable system enables ultrasonic researchers to efficiently prototype different experiments and to incorporate high performance ultrasonic signal and image processing algorithms.**

I. INTRODUCTION

Ultrasonic systems find vital applications, especially in the field of medical imaging and non-destructive testing & analysis. With the current advancements in the modern embedded systems, existing ultrasonic platforms can be further enhanced to build portable standalone system. With the availability of programmable logic devices such as FPGAs and system-on-chips (SoC), it is imperative that these devices can be used to leverage the development of embedded computing systems by virtue of their higher processing capability, low power consumption and compact size; making them ideal for developing portable handheld systems.

In this study, we develop a highly flexible sensor front-end which is interfaced to a high fidelity ultrasonic system-on-chip processing unit. The desired capability of the front-end is derived from the operating frequency range of ultrasonic systems and their end applications. This combination of a programmable analog front-end and a high performance processing back-end system supporting hardware/software (HW/SW) co-design facilitates an efficient, fully controllable and portable hardware platform [1]. This can be employed in applications that demand ease of mobility.

A typical ultrasonic system for testing, evaluation and imaging applications is shown in Figure 1. This system is built with a high voltage Pulser driving high frequency pulses in the range of 20 KHz to 20 MHz through the ultrasonic transducer actuated by a processing element (FPGA or microprocessor).

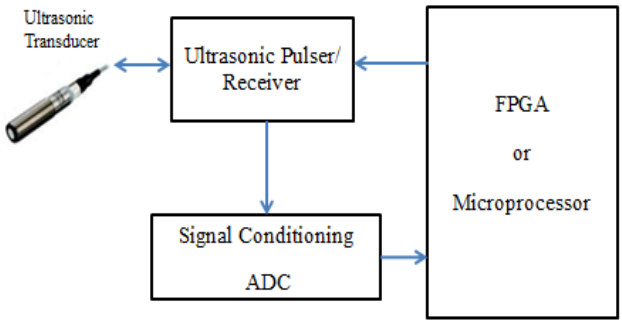

Figure 1 Typical Ultrasonic System

The received reflected signal termed as *echo* is channeled through an ultrasonic receiver and signal conditioning block which converts the raw low voltage analog input to digital sequences which are subsequently processed by the processing element. The design of each component of this system is purely dependent on the application [2]. These basic requirements derived from the intended application challenge the choice of the signal conditioning circuit which consists of a noise attenuator and an amplifier. The data converter chosen must possess the sampling capability as demanded by the application and the received echo signal frequency.

A typical ultrasonic NDE system, as discussed above, is highly limited in its capability by its inherent inflexibility. Hence, any change that needs to be accommodated would result in a significant expense as part of modifying the existing circuitry. In this study, we concentrate on building a highly flexible system by enhancing its capabilities for varied applications. In this proposed system, a fully controllable front-end Pulser/Receiver sub-system is presented. The back-end consists of a Xilinx Zynq SoC

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sub-system providing the capability to process computationally intensive signal processing algorithms [3]. The flexibility built into the front-end has the capability to allow for various beamforming requirements which enable the back-end processor to support various signal processing algorithms including *chirplet signal decomposition* (CSD), *discrete wavelet transform* (DWT), *coherent averaging* and *split-spectrum processing* (SSP) [3]. Additionally, this system finds application in areas where pseudo-random sequences are used [4, 5] to measure certain physical parameters such as distance and speed of a mobile target. The cross-correlation algorithms for pseudo-random sequences can be loaded and executed in the ARM core of the Zynq SoC.

In this paper, Section II describes the proposed system architecture. Sections III and IV detail the Transmit (Tx) channel sub-system & Receive (Rx) channel sub-system implementations respectively. Section V summarizes the evaluation of this system considering typical signal processing algorithms. Section VI concludes this paper.

II. SYSTEM DESCRIPTION

Our ultrasonic testing system comprises of the front-end sensor interface with an associated conditioning block and a back-end processing unit. The front-end hardware, shown in Figure 2, is built with Texas Instruments (TI) LM96550 High Voltage (HV) Pulser, LM96530 Transmit/Receive (T/R) Switch, and LM96570 Beamformer over TX-SDK-V2 evaluation module. Analog Devices analog-to-digital converter (ADC) AD9467 is used for data conversion at 250MSPS through the Native FMC Card [6]. Noise filtering for the received echo is facilitated by the low noise pre-amplifier (LNP) followed by a variable gain amplifier (VGA). Together they provide a maximum gain of 50dB through the receiver.

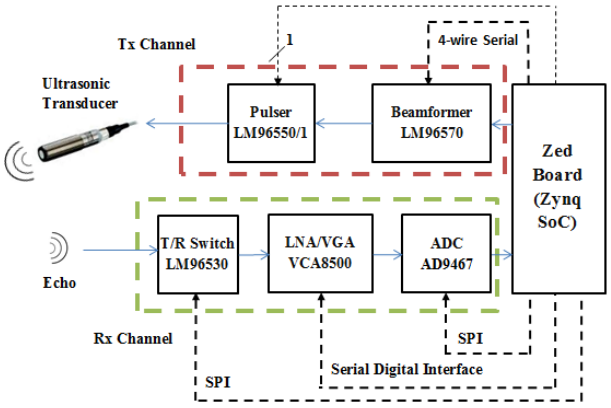


Figure 2 Proposed Ultrasonic System

The Pulser/Receiver sub-system can be broken down into two channels: Transmit (Tx) and Receive (Rx) as marked in Figure 2. The Tx channel consists of a programmable Pulser and digital beamformer. The Rx channel consists of a T/R Switch, LNP, Programmable Gain Amplifier (PGA) and a high-speed ADC.

The back-end processing and control is coordinated by a Xilinx Zynq SoC which combines an ARM dual-core processing unit with an FPGA fabric. The main components of this system are the ARM Cortex A9 CPUs running at 1GHz which support 32-bit advanced ARM instructions [7]. Each processor has its own single instruction multiple data (SIMD) media processing engine (NEON), memory management unit (MMU) and separate 32KB level-one (L-1) instruction and data caches. The Cortex-A9 processor implements the ARMv7-A architecture with full virtual memory support. Previous study shows that ARM processor is a powerful processing device and outperforms some of the existing FPGAs significantly [3].

In the proposed system, each component is configured by the ARM core in Zynq SoC and the system initiation is controlled either directly on the hardware or remotely through the Internet. The sequence of events for the proposed system is presented in Figure 3.

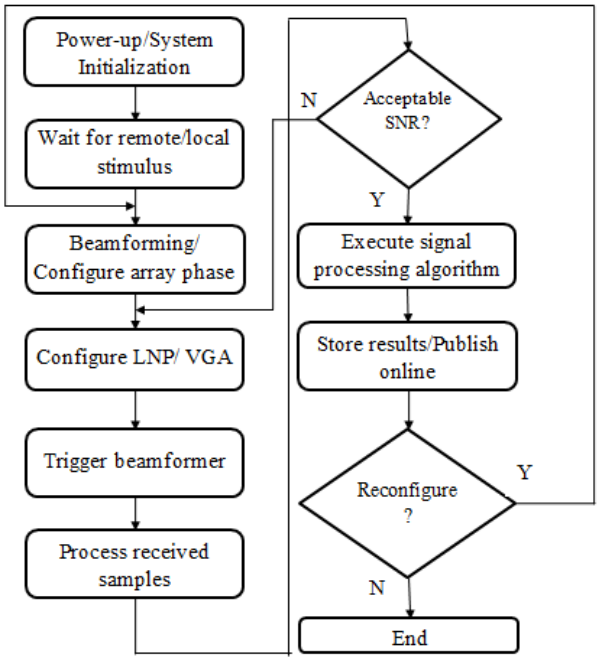


Figure 3 System Process Flow

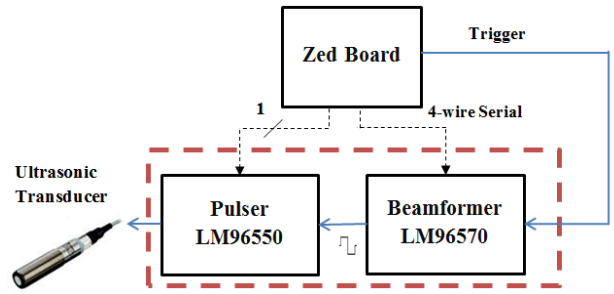
The description of the hardware and the configurable parameters for each activity in the process flow is

explained in the subsequent sections. These activities and transition between activities are controlled completely through the Zynq SoC which incorporates the hardware/software co-design principles. A local computer or personal computing device such as a smart phone, tablet can instigate this process through a wired channel or over the Internet. Considering a diagnostic system comprising of multiple equipment including an ultrasonic evaluation module such as our proposed system can be remotely connected through the internet following the modular concept of *Internet of Things* by applying an ID specific to this unit and executing an internet application for initiating and remotely collecting the processed data.

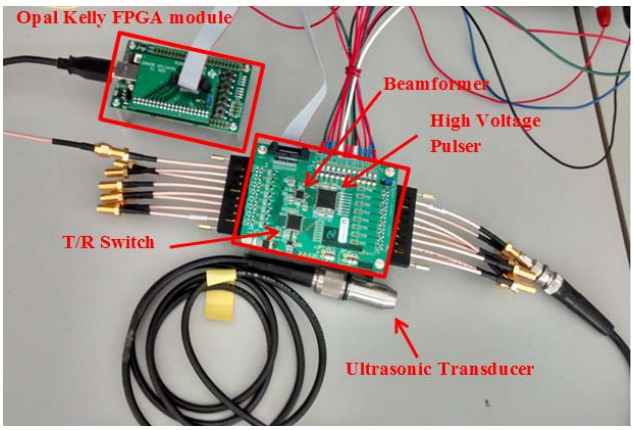
The above mentioned process is generalized for various signal processing algorithms. Upon initiation, the profile for the transmitting wavefront and receiver channel gain are configured. The excitation signal is fired and the received echo signal is evaluated for expected quality by measuring its signal-to-noise ratio (SNR) or the timing parameters. An unacceptable signal is discarded and further re-configurations are enabled till the received echo is acceptable for further processing. These iterations aim at using the optimum reflected signal for accurate imaging. In applications that require imaging multiple zones or layers in 2-D form, the beamforming pattern can be reconfigured immediately following the completion of the previous iteration.

III. TRANSMIT (Tx) CHANNEL SUB-SYSTEM

The Tx channel consists of a programmable Pulser and digital beamformer as shown in Figure 4. On the transmit channel, the Tx beamformer is a programmable device capable of configuring the delay pattern and pulse train required to set the desired transmit focal point up to 64 pulses at 80MHz making it suitable for a variety of ultrasonic applications. This 8-channel digital beamformer generates positive and negative pulses for the high-voltage (HV) Pulser control inputs serving as the on-board sequence generator. The pulse pattern on each channel (CH0 to CH7) is programmed into the internal registers for both positive and negative pulse trains. This pulse pattern can be configured in 2^n steps between 4 and 64 pulses by choosing the appropriate bit depth for each channel. The firing profile for each channel can be controlled by programming the firing delay in discrete steps which provides an accurate timing control for the ultrasonic transducer excitation. Each channel launches this individually programmable pulse pattern with a maximum delay of 102.4µs; adjustable in increments of 0.78 ns or 6.25 ns or a combination of the two. The voltage levels of positive and negative excitation pulses can be directly controlled by the VPP and VNN supply provided to the Pulser IC.



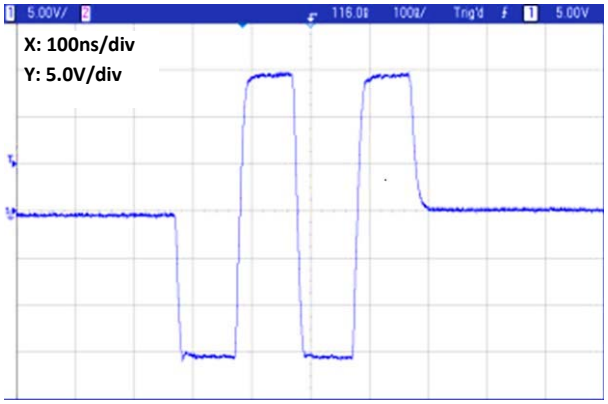
(a)



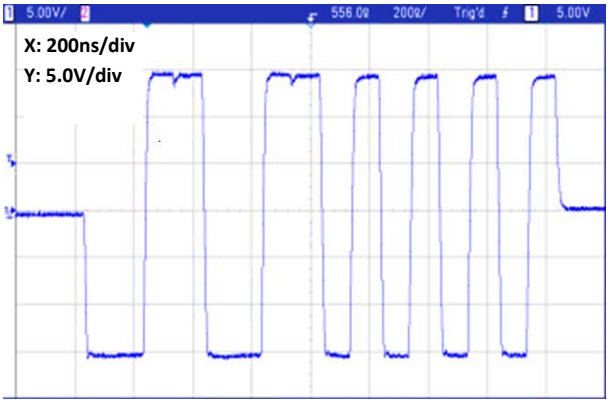
(b)

Figure 4 (a) Tx Block Diagram. (b) Hardware Realization of Tx Channel

The excitation for the ultrasonic transducer is initiated by the controller triggering the TX_EN signal. Based on the chosen pulse train pattern, excitation frequency and repetition rate, the beamformer generates the positive and negative trigger pulses for the Pulser. These are 3.3V synchronization sequence which enables the Pulser to output high voltage signal. A +3.3V pulse on the Pulser positive input (PIN) translates to a +50V at the Pulser output and a +3.3V pulse on the Pulser negative input (NIN) translates to a -50V pulse at its output. This sequence can be varied for each of the 8 channels by programing into the respective registers of the beamformer. This gives us tremendous flexibility in customizing the pulse pattern varying in length from 4 pulses to 64 pulses as shown in Figure 5 (a). The custom pulse trains can be configured to the desired pattern as shown in Figure 5 (b) for applications in pseudo-random sequence generation and analysis.



(a)



(b)

Figure 5 Pulser output at ±15V (a) 4-bit switching pulse pattern (b) 16-bit custom pulse patterns

Our application is expected to operate in the frequency range of 1MHz to 15MHz at ±50V pulses. Typically, multiple transmit focal regions (zones) are scanned for imaging applications. Since the high voltage pulses undergo attenuation as the beam travels further into the target material, the transmit energy is focused gradually deeper into the material. This system outputs high voltage pulses at a very high frequency which makes it imperative to install an isolation barrier for the Rx channel. This is achieved by a T/R switch which acts as a multiplexer and protects the LNP and VGA on the Rx channel from high voltage pulses on the probe transmission line.

In this study, the transmit channel is being controlled by an Opal Kelly FPGA module along with a Texas Instruments ultrasound application software. The Pulser output is configured to support a high voltage pulses. This hardware includes a 4-wire serial interface to the beamformer and a standard serial peripheral interface (SPI) for configuring T/R switch. These interfaces will be controlled by the Zynq SoC providing a dynamic mode control for a reconfigurable hardware platform based on the desired application.

Ultrasonic pulses undergo unequal attenuation due to reflection, refraction and absorption. Hence, the received pulse-echo signals consist of signals spanning a large dynamic range which makes this raw data unsuitable for processing, and further signal gain compensation is applied. Initial compensation is applied to the VGA on the receiver channel. This amplifier varies the voltage gain with respect to time in order to shrink the dynamic range of the echo signal levels. The reflections from the inner layers of the target evaluation material are compensated by applying a higher gain than that for the target surface layers [8]. This process known as time gain compensation (TGC) or depth gain control (DGC) is effectively implemented by the processor employing an adaptive time-gain compensated scan by re-configuring the time delay for the high voltage pulses and the VGA gain for each of the 8-channels independently.

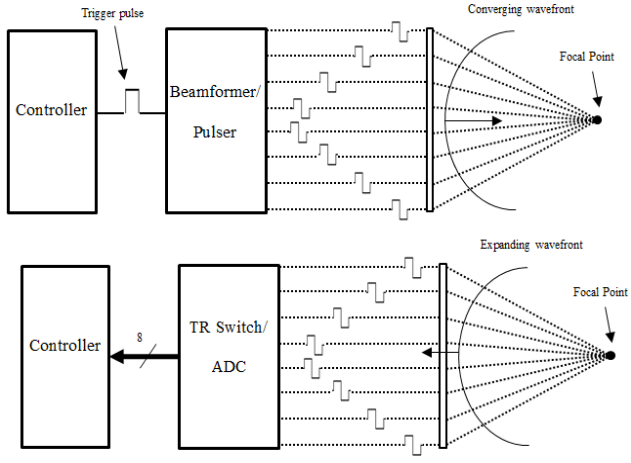
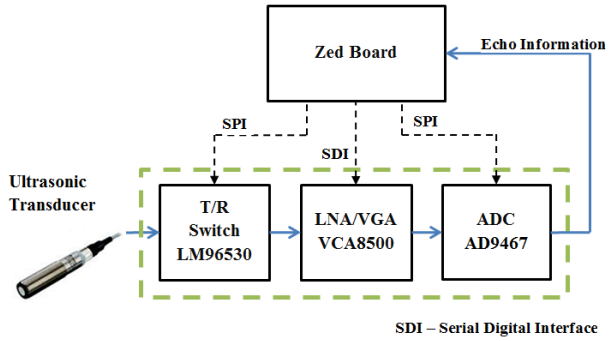


Figure 6 Phased Array Beamforming

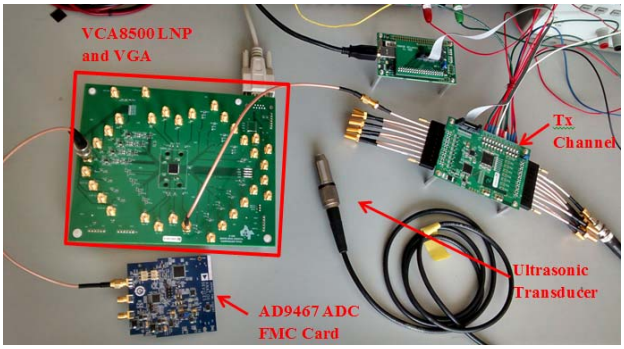
In our current study, a single transducer is used to generate a linear scan by a linear motion in the horizontal direction with a pulse transmitted at discrete steps. Since the motion of the transducer during image acquisition determines the shape of the image, a linear array up to 8 transducers can be effectively employed for a *linear* scan. In a similar manner, an *arc* or a *sector* scan is possible by appropriately positioning the array of transducers [2]. Applications that require a phased array configuration, as shown in Figure 6, can be implemented with ease, as the hardware supports multiple transducers on the Tx and Rx channels with the digital beamforming being presented with programmable accurate delays up to 102.4µs adjustable in increments of 0.78 ns.

IV. RECEIVE (Rx) CHANNEL SUB-SYSTEM

The Rx channel consists of a T/R switch, LNP, VGA and an ADC as shown in Figure 7. In this study, the T/R switch provides an 8-channel programmable receive side interface with each Rx switch channel driven by a HV Pulser that is directly connected to a transducer.



(a)



(b)

Figure 7 (a) Rx Block Diagram. (b) Hardware Realization of Rx Channel

The T/R switch protects the receiver input from voltage spikes due to leakage currents flowing through the switches on Rx channel. These switches can be programmed to allow for different bias currents for the diode bridge network. This is set at 8mA in this application through an external bandgap resistor, R_{BG} = 6.2KΩ in order to minimize the insertion loss [9]. Each T/R switch can be individually programmed ON or OFF allowing for low power operation by selectively configuring desired channels through SPI.

The front-end signal conditioning circuit, mainly the noise floor of the LNP, determines the dynamic range of a signal that can be received. Due to the need for accurately imaging near-field strong echoes with minimal distortion simultaneously with far-field weak echoes, a low noise and large signal handling capability is needed in the front-end, in particular, the LNP. VCA8500 is chosen as the ideal component integrating LNP and VGA. The 8-channel amplifier provides a fixed 20dB gain through LNP and the PGA gain can be digitally controlled via a serial interface. The gain settings supported are 20dB, 25dB, 27dB and 30dB resulting in a maximum gain of 50dB through the VGA block which is equivalent to a voltage gain factor of 316. LNP and PGA are fully differential amplifiers with the internal voltage controlled attenuator (VCA) gain being controlled by an external voltage control input spanning between 0V (maximum attenuation) and 12V (minimum attenuation). The output of VCA8500 is a differential type symmetrically around a fixed common-mode output voltage of +1.65V designated to drive the full-scale 2Vpp to ADC.

Data acquisition through the ADC involves the conversion of the 2-D echo information into a digital format ready for pre-processing. In order to increase the resolution on a scan line or channel, more data needs to be captured and therefore, the obvious way is to use higher sampling speeds on the ADCs for each channel. The rate of data sampling specification for the ADC is determined by the highest frequency of the echo which is to be imaged [2]. A perfect 12-bit SNR or better ADC with a minimum sampling rate of 200MSPS is needed for processing through the Rx channel. This is realized by choosing AD9467 from Analog Devices. The AD9467 is a 16-bit, ADC supporting up to 250MSPS. The AD9467 input is configured as a differential type with ENOB (effective number of bits) of 12 bits at 15MHz effectively providing a resolution of 200uV. The Native FMC Card housing AD9467 is built for a single channel operation which accepts a pair of differential inputs from the VGA. For a phased array configuration, every transducer connected requires an ADC channel and this ADC module needs to be replicated for each channel. However, in this study, only a single channel is used. The ADC output in an LVDS scheme is processed by the Zynq SoC. The advanced SIMD instructions supported by ARMv7-A architecture helps in executing the ultrasonic signal processing algorithms at a very high rate.

V. SYSTEM EVALUATION

The implementation of the proposed system requires a robust flexible processing hardware with the capability of hardware/software co-design, presenting a flexible environment for dynamic re-configuration as is the need for application-independent designs. This device needs to

support interfaces to the front-end devices including the digital beamformer, Pulser, T/R Switch, LNP, VGA and ADC which results in a requirement of high computing power and data storage, thereby, limiting the use of an FPGA or a stand-alone processor core. Our system, therefore, considers the employment of a Xilinx Zynq SoC which houses a powerful ARM core for efficient processing of data received through the ADC.

Each ultrasonic application requires the use of specific signal processing algorithm. The programmable features supported by our system can provide certain leverage for ultrasonic signal processing algorithms which are majorly applied to imaging and nondestructive evaluation of materials [10]. Coherent averaging is a method for improving the SNR of the reflected ultrasonic signals by averaging multiple echo responses over a specific time window. This algorithm relies greatly on the accurate synchronization between the transmitted ultrasonic pulse and the received echo through the ADC. In order to provide accurate results, this hardware presents a very accurate timing control for such an application. The split-spectrum processing algorithm aims at improving the target to clutter ratio of the received echo by minimizing the effect of interference due to multiple scattering in the medium of examination. The implementation of SSP therefore makes use of multiple frequency bands to inspect a target. This is facilitated by programming the center frequency of the desired ultrasonic transducer excitation up to 15MHz on the beamformer and controlling the desired pulse profile. Chirplet signal decomposition algorithm is mainly aimed at extracting the individual echo signals from a clutter of interfering echoes by maintaining the adequate signal quality for estimation of each target material. This algorithm is highly computationally intensive as it requires regenerating chirplets with varying parameters during estimation of the echo signal. With our hardware, the capability to provide a better SNR can be ensured by being able to set the desired Rx channel gain as an additional leverage to this implementation. Discrete wavelet transform is used to compress ultrasonic data, without losing the finer details within the signal such as ultrasonic echoes. The proposed front-end can be used to vary the SNR of the input signal to analyze the efficiency of compression with high signal fidelity.

VI. CONCLUSION

Programmable analog front-end for an ultrasonic hardware presents great possibilities by virtue of dynamic real-time control over the components on the data capture path. This offers performance enhancements by supporting varied applications involving parameter or material evaluation, experimentation and imaging. The dynamic control offered through a robust processing device in this system sets it apart and the capability of analyzing and processing real-time high speed data is a great improvement over the existing systems.

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