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Reconfigurable and Programmable System-on-Chip Hardware Platform for Real-time Ultrasonic Testing Applications

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***Abstract*- Present day ultrasonic signal processing applications such as medical imaging and non-destructive testing has stringent requirements on low cost and portability to provide high quality diagnostics and characterization at real-time pace. Advancements in the field of digital signal processing, embedded computing, and semiconductor technologies, have significantly assisted ultrasound researchers in the development of low-cost, portable, and computationally efficient systems. In this study, a reconfigurable and programmable ultrasonic testing system (RPUTS) is designed and developed to effortlessly test and evaluate a wide variety of ultrasonic signal processing applications. RPUTS integrates a reconfigurable Analog Front-End (AFE) which supports up to 8 transducers suitable for phased-array implementations. The back-end processing is provided by Xilinx Zynq System-on-Chip (SoC) which includes a powerful embedded ARM processor. Zynq SoC manages the overall system configuration as well as the execution of the signal processing algorithms. This study demonstrates the capabilities of RPUTS by realizing a complete ultrasonic testing system which acquires ultrasonic data and performs high-speed 3D compression on the acquired data at real-time rate.**

I. Introduction

Modern ultrasonic systems have several applications in industrial and medical fields. Recent advancements in the field of embedded systems and and system-on-chips (SoCs) have provided ultrasonic researcher to develop portable unit suitable for real-time applications. In this study, an efficient architecture is designed and realized for high performance ultrasonic signal processing applications. This reconfigurable and programmable ultrasonic testing system (RPUTS) includes an analog front-end (AFE) which can be dynamically configured. Furthermore, the reconfigurable system-on-chip (SoC) within RPUTS allows real-time computation and data transfer of acquired ultrasonic data. An experimental application including ultrasonic data acquisition followed by data compression is realized on this system, with the Analog Front-End (AFE) built upon a reconfigurable hardware [1].

Several features such as the incident beam pattern, center frequency of operation, and signal conditioning are to be carefully tuned for optimum performance depending on particular application and the target material being evaluated [2]. Unlike conventional systems, in this study, the components such as noise attenuator, beam controller, and amplifier are selected to allow future upgradability. In RPUTS, a high-voltage, high-speed pulse generator LM96551 [3] is used to excite the ultrasonic transducer. The pulse generator supports up to 15MHz operating frequency. The received echoes are filtered and amplified, which are digitized by the ADC for being processed later by using ultrasonic signal-processing algorithms.

II. RPUTS Architecture

Figure 1 shows the RPUTS block diagram. RPUTS architecture consists five major modules: (i) a Pulser/Receiver sub-system based on TX-SDK-V2 ultrasound transmit/receiver board from Texas Instruments (TI), including LM96551 pulser [3], LM96570 beamformer [4], and LM96530 transmit/receive (T/R) switch [5], (ii) a programmable low noise filter/amplifier and a programmable gain control amplifier VCA8500 [6], (iii) an ADC unit AD9467 FMC Card from Analog Devices [7], which includes AD9517 clock management unit (iv) Step motor driver unit, and (v) Zedboard based on Xilinx Zynq SoC [8]. The first four modules constitute the AFE sub-system of RPUTS. Zedborad is the back-end sub-system. The Pulser/Receiver sub-system has two channels: The Tx channel consisting of the programmable Pulser and digital beamformer, and the Rx channel consisting of T/R Switch, Low Noise Amplifier (LNA), Programmable Gain Amplifier (PGA) and the high-speed ADC.

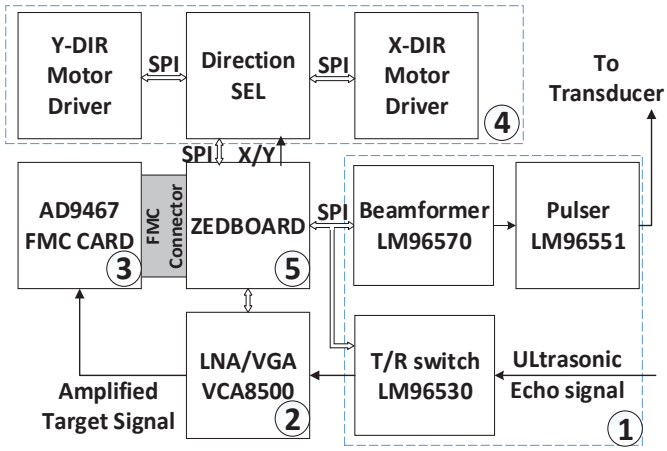

Figure 1. RPUTS block diagram

Zynq SoC within Zedboard is the main controller of the overall system. Zynq SoC consists of dual-core ARM Cortex A9 processors running up to 667 MHz, and a programmable logic FPGAc which are connected over AXI interconnect [8]. The transducer excitation is controlled by the Zynq SoC. Furthermore, the digitized echoes are processed within Zynq SoC.

TX-SDK-V2 evaluation board is used in the system as the ultrasound transmit and receive solution. T/R switch within TX-SDK-V2 provides a programmable receive side interface [5] where each Rx switch channel is driven by a HV pulser that is directly connected to an ultrasonic transducer. The T/R switch protects the receiver input from voltage spikes due to leakage currents flowing through the switches on Rx channel.

The ADC used in this study (AD9467 from Analog Devices) is a 250MSPS 16bit ADC, which is integrated in the AD9467-250EBZ FMC Evaluation Board [7]. The wide frequency range of 50Hz to 250MHz supported by this FMC board is highly suitable for sampling ultrasonic signals. Amplified signal coming from LNA/VGA is sampled by AD9467 FMC card. Then the 16-bit digitized data (LVDS) from ADC is transferred to Zynq SoC through a FMC connector.

In this study, experimental ultrasonic 3D volumetric data is acquired by scanning a transducer over the surface of a steel block test specimen immersed in water. The scanning of the transducer is controlled by two step motors (one for X-direction and one for Y-direction) as shown in Figure 1. Zynq SoC controls the movement of the step motors via SPI bus.

III. System Configuration and Operation

ARM embedded processor within Zynq SoC is responsible for configuring all the components of RPUTS. After configuring the transmitting wavefront profile and receive channel gain, the pulser excitation signal is fired. Then the reflected echoes are captured and assessed for expected quality by determining its signal-to-noise ratio (SNR) and certain timing parameters. Low quality echo signals are rejected and the system is re-configured with modified parameter settings to obtain good quality echo signals that are acceptable for signal processing applications. The VCA8500 can be programmed through SPI to amplify the received echo with gain ranging between 40 dB and 50 dB. Additionally, VCA has a low-noise pre-amplifier with 20 dB gain and a post-gain amplifier which can be programmed to have 4 possible gain settings: 20 dB, 25 dB, 27 dB, and 30 dB [6].

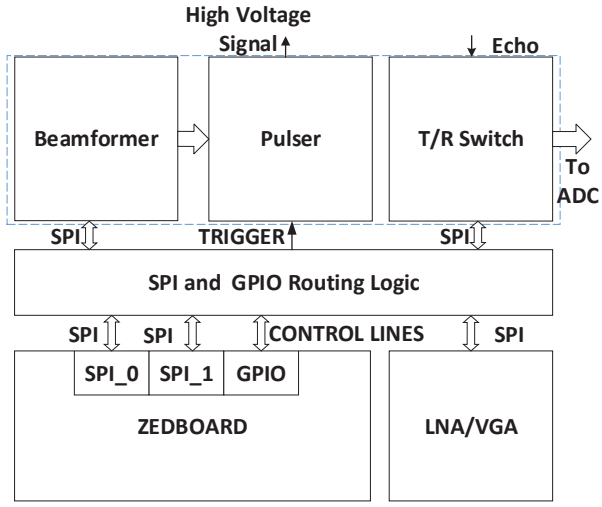

Figure 2. Interface between Zynq SoC and AFE components

Figure 2 shows the interface between Zynq SoC and AFE components. By using serial peripheral interface (SPI) bus, the ARM processor within Zynq SoC configures the AFE components with the beam former first, which generates the pulse pattern, then the variable gain amplifier VCA8500 and finally the T/R switch LM96530 [9]. Beamformer is capable of configuring the pulse train and delay pattern needed to set the transmit focal point up to 64 pulses with a pulse duration of 12.5ns, to suit various ultrasonic imaging and evaluation applications [4]. In addition, the availability of different configurations for beamforming and beam steering helps in realizing several ultrasonic signal processing algorithms such as discrete wavelet transform (DWT) [10], and split-spectrum processing (SSP) [11]. T/R switch can be individually programmed ON or OFF allowing for low power operation by selectively configuring the desired channels through SPI. High voltage pulser is programmed by separate control lines from GPIO as shown in Figure 2.

Figure 3 shows the interfacing between Zynq SoC and AD9467 FMC evaluation board. The SPI adapter block routes the SPI signals to the AD9467 FMC board.

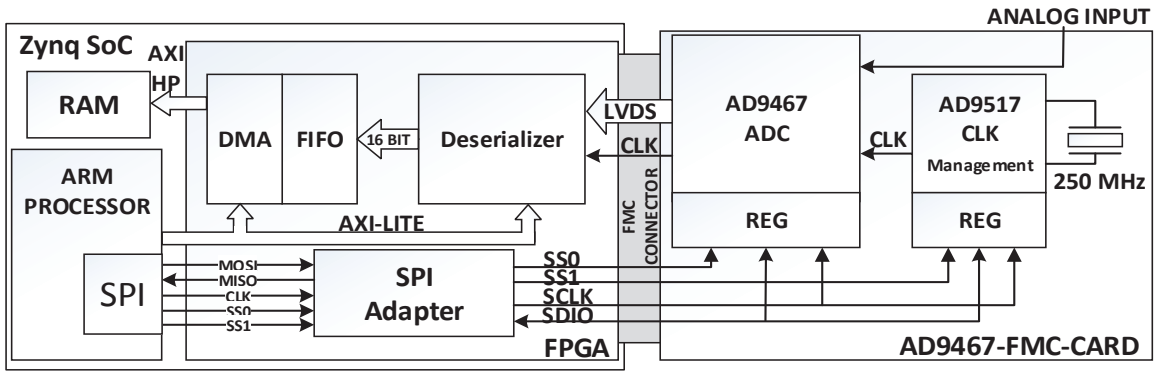

Figure 3. ADC data management in Zynq SoC

The signal coming from the ADC is a serial LVDS signal. In order to make it compatible with Zynq FPGA logic, a de-serializer is used to convert the serial LVDS signal to 16 bit parallel data. The 16-bit parallel data will be buffered and transferred to the RAM by a DMA controller. ARM processor programs the DMA via AXI Lite bus, and ADC via SPI bus. The ARM processor sends a transmit signal to initiate data transfer between ADC and DMA. Once DMA completes the data transfer to the RAM, ARM processor accesses the data stored in the RAM for further processing [12].

RPUTS can be controlled using a computer with a graphical user interface (GUI). The GUI is developed on the eclipse development environment and is written in java. This program runs on a Windows/OS X/Linux machine. It communicates with the system described above, through TCP/IP sockets on an internet connection. The program runs on a tabbed environment where different chips can be configured in their own tabs, before beginning transmission of ultrasound signal. When the "Start Transmission" button is hit, the program sends a packet to the Zynq SoC with the configurations for the AFE components. The Zynq SoC then converts that packet into SPI signals and programs the AFE components. Once the programming is complete, Zynq SoC sends a transmit signal to the beamformer via SPI bus to begin the ultrasound signal transmission. The duration for which the Zynq SoC sends the transmit signal is defined by the GUI user. The transmission ends when the user hits the "Stop Transmission" button. Then a new TCP/IP packet is send to the Zynq SoC, which causes it to stop sending the transmit signal. Now the user is allowed to modify the configuration settings and initiate a new transmission. The flowchart that outlines this process is shown in Figure 4.

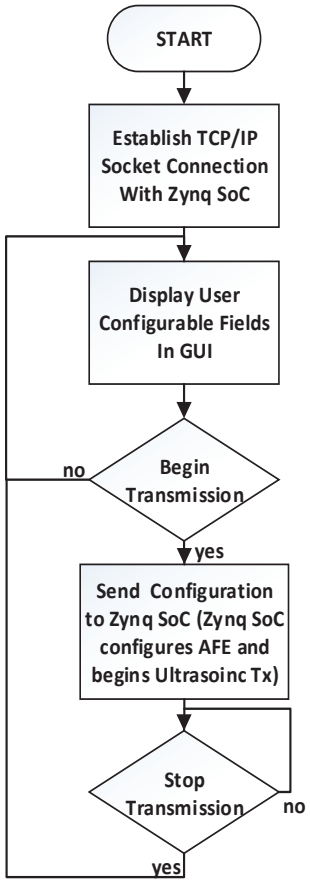

Figure 4. Flowchart of GUI for controlling RPUTS

IV. Performance Evaluation of RPUTS

The RPUTS was evaluated by analyzing the real-time performance of 3D data compression of experimental ultrasonic data using discrete wavelet transform (DWT) method. Figure 5 shows the ultrasound experimental setup for data acquisition, where the surface of the steel block is scanned by using the transducer with the help of two step motors [13], one for movement in X-direction, and another for movement in Y-direction.

The ARM processor within Zynq SoC controls the components on the AFE via SPI and provides excitation for the immersion-type 3.5MHz piezoelectric transducer. In this study, DWT based ultrasonic 3D compression algorithm [13] on is implemented Zynq SoC as a software design using ARM processor, and as a hardware design using programmable logic. A 4-level DWT is applied to the acquired ultrasonic data to produce narrower sub-bands. Those sub-bands with very low energy are eliminated to maximize the compression ratio without affecting the quality of signal reconstruction. 3D compression is performed by successive 1D compression in each of the

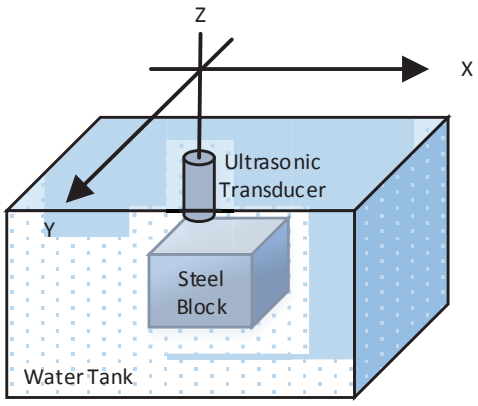

Figure 5. Ultrasonic experimental setup

three axial directions. The 3D ultrasonic experimental data consisting of a volumetric image of 2048x128x128 samples is captured by scanning a 2 inch by 2 inch surface of a steel block test specimen by using a 5 MHz ultrasonic broadband transducer (A3062) at 100 MHz sampling rate with 8 bit resolution [14].

For the software design, the 3D compression with a compression ratio of 98.7% (compressing the volumetric data of 33 MBytes into 0.4 MBytes) is completed in one

minute, indicating the capability of this implementation for real-time ultrasonic imaging applications, whereas the hardware implementation requires only one-fourth of a second, which indicates a very high speed compression suitable for rapid transmission of data in real-time to remote locations via Internet.

V. Conclusion

RPUTS provides a flexible and efficient platform for the realization and testing of computationally intensive ultrasonic signal processing applications. Dynamic reconfiguration of AFE sub-system within RPUTS allows the researchers to conduct several real-time ultrasonic signal processing experiments for NDE. Furthermore, the ARM processor and the programmable logic within Zynq SoC adds flexibility to the system architecture. In this study, the capabilities of RPUTS is analyzed and evaluated by implementing discrete wavelet transform based data compression using 2 different architectural configurations: (i) hardware-only, and (ii) software-only. In hardware-only design, the Zynq programmable logic compresses 33 MB of acquired ultrasonic data into 0.4 MB in 0.25 seconds, whereas in software-only design the ARM processor within Zynq executes the compression algorithm in 1 minute.

Acknowlegdement

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