Reconfigurable Accelerator Design Platform for Ultrasonic Signal Processing and Imaging Applications

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Abstract - Ultrasonic testing and imaging systems have evolved from a basic single transducer system to arrays capable of 3-dimensional scans. These systems need to be flexible and also reconfigurable in order to acquire and process a vast amount of data. The system must also allow for a variety of parameters like the data acquisition rate, signal lengths and processing characteristics which need to be reconfigurable for adaptability to different applications. This study presents a reconfigurable hardware/software co-design system including specific hardware accelerators to acquire and perform ultrasonic signal processing efficiently. For this study, the architecture of the developed ultrasonic system is comprised of two different functional components. One component is specially designed to process the data while the other component gathers, compresses and transfers data which can later be restored and analyzed. For data transfer a simple and consequently efficient real-time operating system and Ethernet connectivity is developed. This is all implemented on the ZEDBoard Zynq SoC for maximum flexibility and performance. The data handling component is built with support for gathering, compressing, reconstructing, and transferring data to other platforms via Ethernet communication. The different variations of the designs allow the system designers the choice of applying the best solution for their specific applications.

Keywords - Signal Processing; FPGA; Reconfigurable Accelerators

I. INTRODUCTION

Many areas of the industry require quality control and nondestructive testing of critical structures for safe operation. Ultrasonic Systems are capable of high precision measurements, imaging, and nondestructive testing and data analysis. To monitor and determine the characteristics of the test subject nondestructively, the ultrasonic echo signal needs to be processed for flaw detection. Different computational intense methods including Split Spectrum Processing (SSP), Chirplet Signal Decomposition (CSD), and Discrete Wavelet Transform (DWT) are shown to be promising for ultrasonic signal analysis [1-12]. In this study, for the specific applications and test setup at hand, the SSP method [1] is of interest for processing the signal, and DWT methodology is of interest for compressing, transmitting, storing, and decompressing the signal for later analysis [6].

Processing large data in real-time using a typical Central Processing Unit (CPU) is difficult to achieve. Consequently, a flexible and reconfigurable system which allows for parallel and distributed computation must be used. In this study a Field Programmable Gate Array (FPGA) fabric is used as a platform to design and test different processing accelerators. For design efficiency a System-on-Chip (SoC) solution utilizing a Zynq SoC from Xilinx [13] was considered as the most suitable platform currently available for the reconfigurable ultrasonic testing and imaging system. The developed SoC based signal processing and imaging system was tested using the SSP algorithm, a well-known and efficient method for ultrasonic flaw detection [1,2]. SSP is computationally heavy because it requires subband decompositions using several discrete Fourier transform operations in parallel. Another practical signal processing application of the developed SoC platform is data compression and reconstruction using DWT. Both SSP and DWT-based data compression and reconstruction were implemented on the ZEDBoard Zynq SoC [14] in order to demonstrate the developed system flexibility, configurability and computational efficiency. A block diagram representation of the overall reconfigurable ultrasonic system is shown in Figure 1.

![Figure 1. Block Diagram of Reconfigurable Accelerator Design Platform for Ultrasonic Testing](image)

A. SSP Method

Ultrasonic signal processing is designed to produce a more valuable and easy to understand outcome. This signal processing can be performed many different ways. SSP is a common way in which ultrasonic flaw detection [1] is realized using Fast Fourier Transform (FFT) and window multiplication in frequency domain (known as the subband decomposition) followed by inverse FFT (iFFT). The flow of operations for this calculation using 8 subbands windows is shown in Figure 2.

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FFT is used for calculating the discrete Fourier transform of a time-domain signal efficiently. For large data sets, FFT and iFFT calculations are computationally intensive. Therefore, FPGA/DSP fabrics are most suitable for efficient implementation of FFT and iFFT.

**B. Data Compression and Reconstruction Method**

Ultrasonic 3D imaging requires the echo response from many different points of the test subject. For efficient data transfer and storage, a real-time compression and reconstruction system must be realized. In our previous research [8] it has been determined that for ultrasonic flaw detection and material characterization, the signal contains energy in only very specific frequency bands. DWT is used to isolate these frequencies, thereby, compressing the data. DWT signal decomposition of a typical ultrasonic signal is shown in Figure 3. This figure is generated using the processing block diagram shown in Figure 3. A filter and down sampling network is designed to isolate critical frequency bands and to extract them from the original signal. Figure 2 also indicates that only signal paths in color are isolated and stored while grayed out signal paths are discarded. The isolated frequencies can be later reconstructed (decompressed) into the original signal (see Figure 4). For compression the decomposed signal components of interest are those that comprise Y LLL and Y LLHH as shown in Figure 3. The remaining signal components are low power and therefore, can be removed. By saving only the values of Y LLL and Y LLHH frequency bands a compression ratio of 81.25% can be achieved while maintaining a 98.31% correlation after reconstruction [8].

With the signal compressed, the signals will eventually need to be reconstructed when processing and analysis of the signal is requested. In order to do this the compressed signal needs to be up scaled, combined and the removed frequency bands reinserted. Since the information in certain frequency bands not stored was negligible, those frequency bands can be reinserted with an amplitude of 0. The operation of this is similar to that of compression but in reverse. The signal reconstruction is shown in Figure 5.
another FFT that is now configured in the inverse direction to operate as an iFFT. This transforms the frequency domain signal into a time domain signal for each subband.

All 9 FFTs in the system, 1 forward FFT and 8 inverse FFTs, have identical parameters to maintain matching approximations and latencies. The FFTs have a transformation length of 2048 words with the possibility of expanding to 65,536 words. The architecture choice for this design was Radix-4 calculation as it allowed a great balance between latency, maximum frequency, and resource utilization. To keep FPGA resources down, the design utilized DSP slices for the multiplication and for portions of the FFT and iFFT calculations. This allows for spare resources on the FPGA fabric for further logic implementation. The subband windows are implemented in the design using Gaussian windows that overlaps by 75%. This window and overlap percentage were chosen as previous experimentation concluded that it offers the best performance for ultrasonic signal analysis.

Computational speed of a system needs to be very fast in order for the system to process the arriving signal in real-time. Measurements were taken of the hardware execution time for a data stream of 2048-word length. Another measurement was taken for the overall hardware/software design execution time for the same data stream. The total amount of time that it takes for the system to transfer data from the DDR3 memory, perform SSP operation and record the result back to the DDR3 memory takes 177.22 microseconds. With the test subject containing ultrasonic data set in a 128 by 128 grid results in a total of 16,384 sets of calculations. Therefore, a SSP calculation for the entire test subject can be completed in approximately 2.9 seconds. This is an acceptable speed for real-time processing since in order for the system to be able to gather that much data the ultrasonic transducer needs to physically move to all 16,384 test points.

B. DWT Compression/Decompression Accelerators

For the DWT compression circuit, two different methods were implemented: A system of discrete adders and multipliers and a system of adders and shifters. Both methods utilized the same type and levels of filter stages with the only difference being how each individual stage calculated the result. The system utilizing discrete adders and multipliers permits the designer to implement different coefficients quickly. The drawback to this approach is that vast amounts of resources are used as the multiplication is resource intensive. The coefficients used in this design where the most optimal values were previously determined during experimentation [8]. The multipliers were implemented utilizing DSP slices and again utilizing FPGA fabric for comparison of performance characteristics.

The second method replaces the multipliers with a series of shifters and adders. By utilizing this method, the resources are brought down drastically and computation time is decreased as the individual data paths have decrease from the full multiplier and adder combination to just buffers, and adder combination. The drawback to this approach is that implementing different coefficient values requires redesigning the system since the coefficients are hard designed into the shifters and adders combination. The shifter and adder combination used in this design where the most optimal values previously determined during experimentation. The method for designing this system was to include buffers of appropriate size for each intermediate stage.

For the DWT decompression (aka reconstruction) circuit, two different methods were also implemented: A system of discrete adders and multipliers and a system of adders and shifters. The basic filter design for both methods are identical to that of the DWT compression circuit with the only changes being in the coefficient values. For the system utilizing discrete adders and multipliers this change was simple to implement since the coefficient in each multiplier was quickly changed to the correct value for reconstruction. Similarly, the shifters and adders where implemented utilizing previously determined values for DWT coefficients. The main differences between the DWT compression circuit and the DWT decompression circuit is what happens outside of the filter block stages. Instead of down sampling the signal in the DWT compression circuit, in the DWT deconstruction circuit the signal is up scaled. The process for upscaling was performed similarly to the down sampling method. FIFO buffer blocks where used to capture and store the signal.

The ultrasonic signal data handling system is a system purposefully built for Data Retrieval, Data Compression, and Data Reconstruction. This system utilizes the DWT Compression and DWT Reconstruction IP cores. In addition, the system is expanded to include the AD9467 IP core provided by Analog Devices to read in the data from the ADC. Data is stored on the DDR3 memory and is transferred to and from the DWT Compression and DWT Reconstruction IP cores while data is received from the AD9467 IP core. All data transfers are performed by DMA IP cores. In addition to the hardware implemented in the FPGA fabric and DSP slices, the system also utilizes a single ARM core to initialize the system and configure all of the DMA IP and AD9467 IP cores. An Ethernet transceiver is utilized on the ZEDBoard to provide the physical.
layer for the Ethernet protocol. And finally a PC is connected via an Ethernet cable to transfer data back and forth (see Figure 1).

An area that can be more demanding on a system performance is during capture and saving massive data. In order to minimize the amount of storage space the ultrasonic signal is compressed. Measurements were taken of the hardware execution time for a data stream of a 2048-word length. Another measurement was taken for the overall hardware/software design execution time for the same data stream. The total amount of time that it takes for the system to transfer data from the DDR3 memory, perform the compression and store the result back into the DDR3 memory takes 53.19 microseconds for the pipelined implementations and 72.08 microseconds for the non-pipelined implementation. With the test subject containing ultrasonic data set in a 128 by 128 grid results in a total of 16,384 sets of calculations. Therefore, the compression calculation for the entire test subject would be completed in approximately 0.872 seconds for the pipelined implementations and 1.18 seconds for the non-pipelined implementations. This is an acceptable speed for real-time processing, since in order for the system to be able to gather that much data the ultrasonic transducer needs to physically move to all 16,384 test points.

Compressed data eventually will need to be reconstructed during processing. Measurements were taken of the hardware execution time for a reconstructed signal of 2048-word length. Another measurement was taken for the overall hardware/software design execution time for the same data stream. The total amount of time that it takes for the system to transfer data from the DDR3 memory, perform the reconstruction and record the result back to the DDR3 memory takes 31.90 microseconds for the pipelined implementations and 70.26 microseconds for the non-pipelined implementation. Therefore, the compression calculation for the entire test subject (128 by 128 grid results in a total of 16,384 sets of calculations) can be completed in approximately 0.523 seconds for the pipelined implementations and 1.16 seconds for the non-pipelined implementations. This is an acceptable speed for real time since any further processing operation will take at least this long if not longer to perform.

### III. CONCLUSION

With the use of reconfigurable logic and parallel computation a flexible, efficient and complex ultrasonic system can be built. For this study, the system is built around the Zynq SoC. One system is specifically built to process the data and another system to gather, compress, store and/ or transfer the data which can later be reconstructed. These systems provide a powerful platform to experiment and build the next generation of ultrasonic systems. The processing system is built with support for real-time split spectrum processing to be performed on the ultrasonic signal. It also leaves the user the flexibility to modify key parameters to tune the system to any specific application. The data handing system is built with support for gathering data, compressing data, reconstructing data, and transferring data to other platforms via Ethernet communication. The different variations of the designs allow the users the choice of applying the best solution for their specific application.

### REFERENCES


