Ultrasonic Signal Acquisition and Processing Platform based on Zynq SoC

Boyang Wang and Jafar Saniie
Department of Electrical and Computer Engineering
Illinois Institute of Technology, Chicago, Illinois, U.S.A.

***Abstract* – Ultrasonic testing systems have been widely used in medical and industrial fields, demanding strict requirements for processing speed and re-configurability of the hardware system. This paper presents a prototype of a reconfigurable, high performance, low cost and real-time Ultrasonic Signal Acquisition and Processing (USAP) platform based on Zynq System-on-Chip (SoC). The USAP platform consists of five major components: Multi-level voltage power supply; High voltage pulse generation; Ultrasonic signal acquisition; Sampling control unit and Digital signal processing module. The system uses Xilinx Zynq SoC as main processor and controller. It combines both ARM processor and field-programmable gate array (FPGA) on the same chip, which makes the system capable of doing complex system configuration and performing high speed data processing. With this arrangement, the developed system is highly reconfigurable, where software and hardware configuration can be changed on both ARM and FPGA. This paper presents a system design flow of a complete ultrasonic testing system which is capable of acquiring ultrasonic data and performing advanced signal processing algorithms in real-time.**

Keywords: Ultrasonic System, Zynq SoC, FPGA, Signal Acquisition and Processing

I. INTRODUCTION

Ultrasonic signal acquisition and processing systems have strict requirements and are challenging when used to perform real-time signal acquisition and processing. When designing an ultrasonic testing system, many factors like processing speed, system flexibility, portability and system complexity are crucial. Hard core processors like ARM are capable of doing complex operations, which include communicating with other devices, controlling peripherals like stepper motors, OLED display, etc. However, ARM lacks the capability of receiving and processing high frequency data in real-time. FPGA is fast and reconfigurable making it suitable for high speed data acquisition and signal processing. On the other hand, FPGAs are not the best for implementing complex communications and control operations. Zynq System-on-Chip (SoC) [1] contains both ARM processors and FPGA fabrics, which facilitates a highly desirable solution for ultrasonic testing. This paper focuses on presenting an ultrasonic signal acquisition and processing platform based on Zynq SoC.

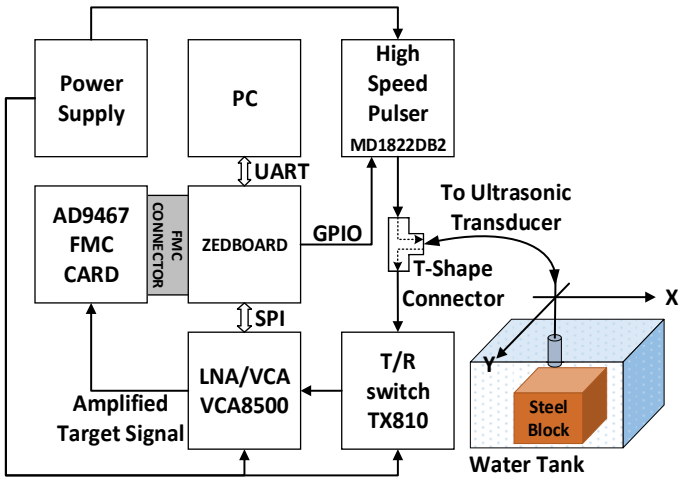

Figure 1. Ultrasonic Testing System Block Diagram

The proposed ultrasonic signal acquisition and processing (USAP) platform are composed of five major parts, which are, Multi-level voltage power supply, High voltage pulse generation, Ultrasonic signal acquisition, Sampling control unit and Digital signal processing module.

Figure 1 displays the overall block diagram of the USAP platform. The system uses a Zedboard [2] as a main control unit which is a Zynq SoC based development board. The Multi-level voltage power supply consists of two boards: AN-H59DB1 development board [3] for the high voltage supply and TSW2200EVM [4] for low voltage supply in the system. A high speed ultrasonic pulser MD1822DB2 development board [3] is used to generate high voltage ultrasonic pulses. The generated pulse is fed to the transducer. In order to be able to scan the 3D objects, the transducer is positioned above a water tank and it can be moved along two axes by using a mechanical setup. The system has a TX810 evaluation board [6] as a Transmit/Receive (T/R) switch. The output of T/R switch is connected to an amplifier board called VCA8500. The amplified signal is then being digitized and sampled by AD9467 FMC card. The sampled data is buffered and transmitted to the Zynq SoC in the format of Low-voltage differential signaling (LVDS), Zynq SoC performs signal processing algorithms on the captured signal.

978-1-4673-9985-2/16/$31.00 ©2016 IEEE

Section II of this paper describes the hardware platform and explains the system setup for obtaining ultrasonic data. Section III describes the architectural advantages of implementing high speed signal processing on Zynq SoC. Examples of signal processing procedures are also given in this section. Section IV concludes this paper.

II. SYSTEM IMPLEMENTATION

The USAP platform has Zedboard as its central control and processing unit of the system. Zedboard is a low-cost development board based on Xilinx Zynq-7000 which integrates the ARM based processor with an FPGA. The ARM processor on the Zynq SoC is primarily used to control the overall behavior of the system. Various peripherals and connectors available on the Zedboard makes it easy to implement an onboard graphical user interface and also to interact with additional devices. With Signal processing logic and Direct Memory Access (DMA) implemented in FPGA, researchers can design fast signal processing without hampering the ARM processing resources. Another advantage of using Zedboard is that the program of the system can be loaded directly from an SD card. ARM processor is being programmed first and subsequently it initializes its peripherals and FPGA on the chip. After initialization is done, the processor will start to run user's program. This makes the system more portable and reliable.

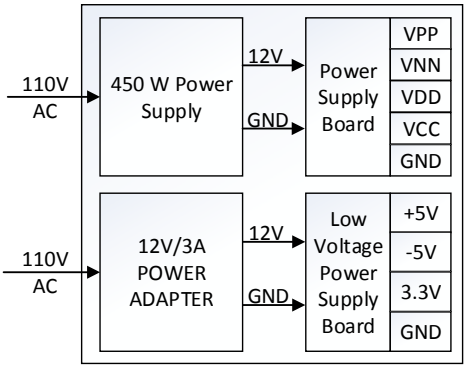

Figure 2. Power Supply Configuration

Figure 2 shows the power supply configuration of the entire system. AN-H59 development board is a high voltage DC/DC converter which is used to power the high speed ultrasonic pulser (MD1822DB2). It can provide up to +90V for V_{PP} and as low as -90V for V_{NN}. V_{PP} and V_{NN} are two very important voltage inputs for the high voltage pulser. They determine the maximum and minimum voltage limits for the ultrasonic pulse. AN-H59 development board also provides a +10V voltage supply for V_{DD} and a +3.3V for V_{CC}. AN-H59 development board draws power from a 450 W desktop computer power supply. Another power module called TSW2200 evaluation module provides a multiple low voltage power supply, including +/-5V and 3.3V for T/R switch (TX810EVB) and the amplifier board (VCA8500BOARD). TSW2200EVM and Zedboard draw power from 12V/3A AC/DC adapter.

The MD1822DB2 development board is a single channel high speed pulser, which is used to generate high voltage ultrasonic pulse. The on-board CPLD-programmable logic circuit can generate an accurate high speed and high voltage pulse. A single trigger signal given by Zynq SoC is used to synchronize the output waveform. The generated ultrasonic pulse is sent to an ultrasonic transducer via SMA connector. The transducer transmits the high voltage pulse toward a specimen under testing and the acoustic reflection termed as "echo" is then picked up by transducer. The echo signal coming back from the target specimen contains the desired information. The received signal is transmitted to TX810 evaluation board. This board is an 8-channel, current-programmable transmit/Receive (T/R) switch. The captured ultrasonic signal contains both transmitted high voltage pulse and low voltage echo signal. The high voltage pulse can be up to 100V, so the target echo is basically buried by the high voltage pulse. Also, high voltage signal has the potential of damaging the receiving circuit. T/R switch is used to clamp the high voltage pulse to a certain voltage and protect the amplification and sampling circuits.

VCA8500EVB is an evaluation board with a variable gain amplifier. This variable gain amplifier is adjustable through SPI interface which can be easily configured by Zynq SoC. The amplifier is composed of a 20dB low noise amplifier (LNA), attenuator, post gain amplifier (PGA), and a low pass filter (LPF). LNA is a low noise component with a fixed gain of 20dB. The attenuator is controlled by an input voltage varying from 0V to 1.2 V, which can be used as a continuous gain control. PGA and LPF can be configured through SPI interface to change the gain and bandwidth. A fully configurable amplifier makes the system more flexible.

The amplified signal will be sampled by the high speed ADC on AD9467 FMC card. AD9467 FMC card has two chips on board, AD9467 is the high speed ADC, and AD9517 is the clock management chip. The input frequency to the clock management chip is 250 MHz and the output frequencies varying between 50Hz and 250 MHz is fed to the ADC chip. In the system that we build, the ADC is configured to sample the signal at the frequency of 250 (Mega-Sample per Second) MSPS, each sample is 16 bit. The sampled data is sent to the Zynq SoC in the format of LVDS. ARM processor cannot receive a serial signal at the rate of 250 MSPS. A hardware logic on FPGA is used here to deserialize the high speed LVDS signal. The deserialized signal is then transmitted to the RAM through a DMA. Details of interfacing this high speed ADC with Zynq SoC is carefully described in a recent paper [7]. Figure 3 shows the USAP platform designed and evaluated for this study. All the components are connected as was described in the Figure 1.

A simple user interface is implemented using OLED display and push buttons on the Zedboard. Once the system is powered up, it loads the hardware configuration for FPGA and executable software for ARM processor from the SD card. Then the ARM processor initializes the system and a "System Ready" message is displayed on the OLED screen. This notifies the users the completion of successful initialization. With the user interface, users can have 3 options from the menu. They are: moving the stepper motor manually; capturing one set of ultrasonic data and starting one complete ultrasonic testing procedure. Moving the stepper motor manually allows the user to put the transducer on a proper positon before the start of testing.

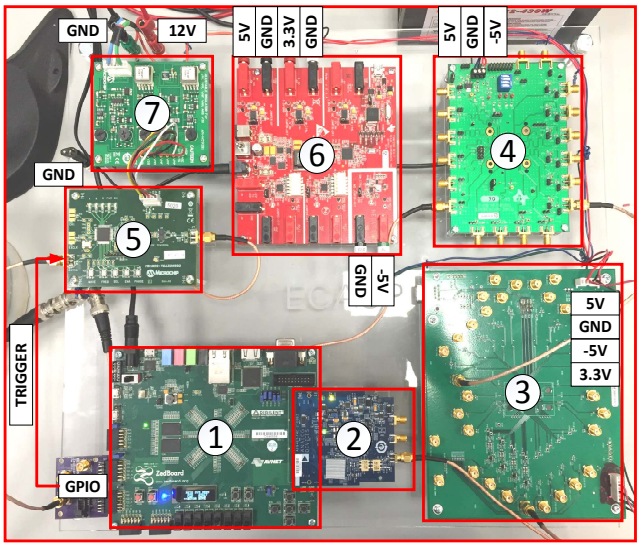

Figure 3. System Components Integrated to Perform Evaluation. [1 Zedboard, 2 AD9467 Evaluation board, 3 VCA8500 Evaluation board, 4 T/R Switch, 5 MD1822DB2 development Board, 6 TSW2200 low voltage power supply, 7 AN-H59 high voltage DC/DC converter]

Two stepper motors enable the system to scan 3D objects other than just testing one single A-scan. Figure 4 shows an A-scan obtained by the system described in this paper. The system block diagram in Figure 1 also illustrates the test setup of the system. Two stepper motors are used to move the transducer on X and Y directions to collect multiple A-scans. The stepper motors are driven by two motor drivers. Through SPI interface, Zynq SoC can precisely control the movement of the transducer to perform B-scan on the top surface of target specimen. Figure 5 illustrates the moving trace of a B-scan; the system will perform one A-scan on each point in the figure.

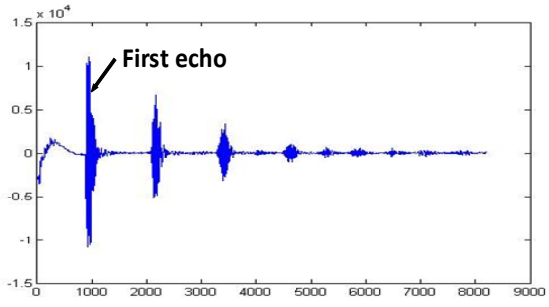

Figure 4. A-scan from the target specimen

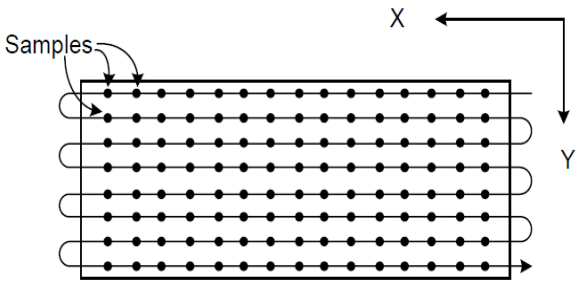

Figure 5. Ultrasonic B-scan scanning pattern

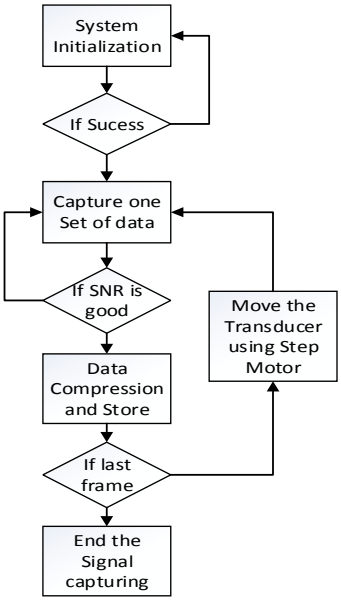

Figure 6. Ultrasonic Test Flow Chart

Figure 6 shows the flow chart for obtaining a complete B-scan from the target specimen. After the initialization, the system will start to perform A-scans on the target specimen. Signal to noise ratio (SNR) of each A-scan is computed by the system to differentiate the good signals. If the obtained signal is a valid A-scan, the stepper motors will move the transducer to the next location. The testing procedure will end when all the points in Figure 5 are tested. Each A-scan contains 8192 samples with 16 bit resolution. This is a huge amount of data to be stored on an embedded device. So a compression algorithm is required in this situation. An algorithm is developed to compress the signal to a very condense format is presented in another paper [8]. The compression ratio can approach 81% which means that the compressed data only take 19% of the original space. The compressed data can be either stored in the Zynq SoC for further processing, or it can be sent over the Ethernet or UART to other devices. In the current system, the data is sent over the UART to a PC, the PC runs a script in MATLAB to receive and plot the data. The result in Figure 4 is one sample test output using the USAP platform

III. SIGNAL PROCESSING

Zynq SoC contains both ARM processor and FPGA on the same chip, which makes the system flexible, efficient and easy to extend. The ARM processor communicates with FPGA using advanced extensible interface (AXI). AXI is targeted at high performance, high clock frequency system designs. Figure 7 shows the hardware and software co-design of signal processing logic. Signal processing logic is implemented in hardware description language (HDL). Direct memory access (DMA) is used to make data transfers between memory and hardware logic. The ARM processor directly controls the hardware logics and DMAs through the AXI bus. The DMA loads the data from the RAM and sends it to the hardware logic to be processed. Once the signal processing is done, the processed data is

transferred back into the RAM. ARM processor can access the RAM for further operations like formatting and transmitting the signal to other devices.

A compression algorithm based on DWT is applied to the captured signal. The hardware and software co-design of this compression algorithm based on Zynq SoC is presented and its performance is evaluated in another paper [9]. This paper shows that the hardware and software co-design can achieve a better performance. The research team at ECASP lab has developed several real-time signal processing algorithms that can be executed using the USAP platform. These algorithms include ultrasonic target detection using split-spectrum processing and neural networks [10], and NDE applications of compressed sensing, signal decomposition and echo estimation [11].

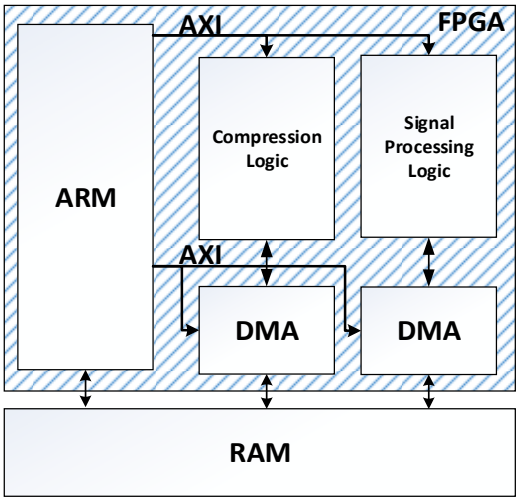

Figure 7. Ultrasonic Signal Processing Setup

IV. CONCLUSION

The USAP platform presented in this paper provides an effective and flexible solution for ultrasonic signal acquisition and processing based on Zynq SoC. The ARM processor on the Zynq SoC enables many complex operations and the FPGA on the Zynq SoC can be customized to accelerate the signal processing speed and extend the complexity of the system. Therefore, system designers and researchers can implement any real time ultrasonic signal processing based on this existing platform by implementing new software on the ARM processor, and new hardware configuration on FPGA. Zedboard can also be configured to use UART or Ethernet communication protocols, which make it convenient to realize real-time control and data transmission on the system. The entire system is assembled on a dedicated acrylic sheet which makes it more portable and easy to use.

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