Software Defined Ultrasonic System for Communication through Solid Structures

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***Abstract* – RF signals are commonly used as a carrier signal in wireless communications. In some situations, like underwater, underground, closed containers or even intra-body, ultrasonic signal is a better carrier signal because RF signal attenuate very fast in these types of channels. Therefore, it is our objective is to assess the capability of using ultrasonic waves as a carrier waveform for communications. Ultrasonic signal is a type of waveform which has a frequency higher than 20 kHz. In this study, a ZYNQ System-on-Chip (SoC) platform is used to conduct ultrasonic communication experiments. This system consists of a transmitting transducer and a receiving transducer operating at MHz range frequencies. The transceiver unit operates using In-phase and Quadrature (IQ) modulation. With IQ modulation, different modulation schemes such as quadrature amplitude modulation (QAM), phase shift keying (PSK) can be readily implemented on the platform without modifying the hardware setup. Experiments are conducted in solid channels with various shape, material and size to explore the ultrasonic communication feasibility in diverse environments. Performance of different modulation methods are discussed and compared in this paper.**

Keywords–Ultrasonic Communication, Software Defined Radio, I/Q Modulation

I. INTRODUCTION

Ultrasound is a type of mechanical wave at a frequency beyond 20 kHz which is the maximum frequency the human can hear. Ultrasonic signals have been widely used in medical and industrial areas for diverse types of applications. Ultrasonic communication uses the ultrasonic signal at the frequency of 20 kHz to 20 MHz as the carrier of information to conduct communication [1]. The ultrasound signal is seldom used for information transmission because it attenuates, scatters, disperses and reverberates in the channel. In certain environments like underground, underwater or even intra-body [2, 3], conventional radio frequency communication is not applicable since the media have high attenuation to RF signals. Researchers show that using ultrasonic signal for communication will have unique security compare to other forms of communication [4, 5]. This paper presents the feasibility of using ultrasound as the carrier of the information. In this study, Piezoelectric transducers are used to generate and receive ultrasonic signals. A platform based on the Field Programmable Gate Array (FPGA), high speed data and signal converters, amplifiers, and transducers are assembled to conduct ultrasonic communication experiments. Experiments are conducted in solid materials with different channel type, shape, and sizes. The objective is to design and examine a reliable system for the ultrasonic communication in solids having diverse physical and geometrical configurations. Section II describes the background of using IQ modulation in Software Define Radio (SDR) systems. Section III introduces the hardware configuration for carrying ultrasonic communication experiments. Section IV presents two test setups and result of modulation and demodulation of using PSK and OOK modulation methods. Section V concludes the paper.

II. BACKGROUND

A critical processing component of SDR is In-phase and Quadrature (IQ) modulation. IQ modulation is an efficient way to transfer information and is easier to be implemented on the digital platform such as FPGA. Also, with IQ modulation, one can implement a variety of Analog and Digital modulation methods. Figure 1 shows the block diagram of the IQ modulation and de-modulation.

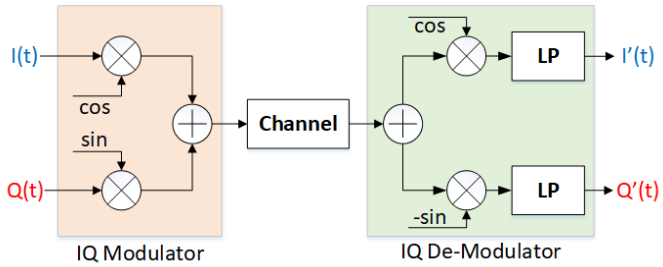

Figure 1. IQ Modulator and De-Modulator Block Diagram

In IQ modulation, in-phase component is multiplied by cosine carrier and quadrature component is multiplied by sinusoid carrier. The modulated signal is the summation of these two products. The de-modulation procedure is found by multiplying the received signal with both sinusoid and cosine waves generated by a local oscillator at the same frequency. This will shift the baseband signal from carrier frequency back to low frequency. It will then be filtered by a low-pass filter to recover the information.

III. HARDWARE PLATFORM

To conduct ultrasonic communication experiments, we considered a ZYNQ based Red-Pitaya system which is capable

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of sampling and reconstructing signals at 125 MSPS. This system consists of two ADCs and two DACs which makes it ideal for SDR based ultrasonic communication in MHz frequency range. Both high speed ADC and DAC can operate at 125 MSPS, and have a 3 dB bandwidth of 50 MHz and resolution of 14 bits. ZYNQ SoC manufactured by Xilinx consists of dual core ARM A9 processors and a FPGA fabric. The FPGA serving as the peripheral of the ARM processor can expand the system IO and accelerate the algorithm realization. The high bandwidth between the FPGA and ARM processor allows the user to design high performance reconfigurable systems.

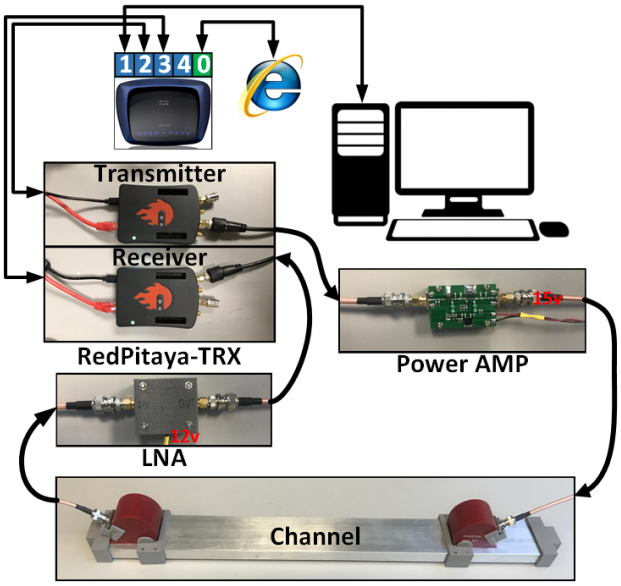

Figure 2. Ultrasonic Communication System Diagram

Figure 2 displays the system diagram of the ultrasonic communication experimental platform. The system contains two Red-Pitaya boards, both are configured as transceivers which have full capability of transmitting and receiving RF signals up to 60 MHz. In this test setup, the upper device is used as the transmitter. The baseband signal generated by the host computer will be sent to a transmitter through the ethernet cable. On the FPGA, this baseband signal is processed by a digital up-converter (DUC) and sent to the on-board 125 MSPS DAC. The output is connected to a power amplifier to increase the driving capability. The amplified signal will be converted to an ultrasonic wave by a piezoelectric transducer and travel through the channel. The signal will be picked up by the receiving transducer. Due to attenuation, reflection and refraction in the channel, the received signal is weak and must be amplified. Therefore, the received signal is amplified by a 20 dB Low Noise Amplifier (LNA) and sampled at 125 MSPS ADC. The sampled signal is processed using a digital down-converter on the FPGA to recover the baseband signal.

Figure 3 shows the block diagram of the Digital Up Converter (DUC) and the Digital Down Converter (DDC) on the FPGA. The red arrows in the figure represents high speed AXI4-Stream bus interface. Green arrows represent AXI4-Lite bus interface, it is a general purpose read and write bus interface which allows for low speed data transmission between peripheral and processor. The cascaded integrator-comb (CIC) compiler is a Xilinx LogiCORE IP core which provides the ability to design and implement AXI4-Stream-compliant CIC filters [6]. CIC multi-rate filters are commonly used for implementing large sample rate changes in digital systems. In SDR systems, the carrier frequency is much higher than the baseband frequency. A CIC filter is necessary for both DUC and DDC subsystems to match the sample frequency of the carrier signal and baseband signal. The Direct Digital Synthesizer (DDS) compiler is a Xilinx LogiCORE IP core which is used to generate precise Sinusoid and Cosine waveforms for DUC and DDC [7]. The DUC implements I/Q modulator and the DDC implements the I/Q de-modulator according to the diagram shown in Figure 1.

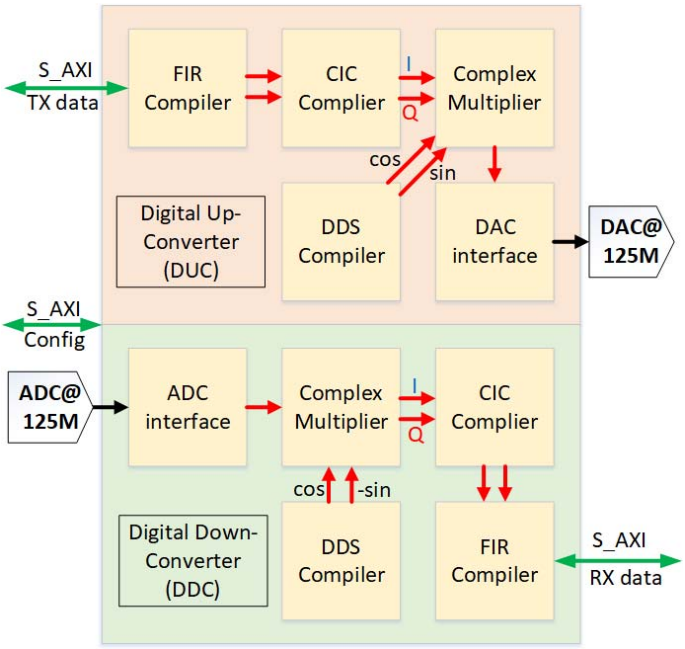

Figure 3. Block Diagram on FPGA

Figure 3 also shows the benefit of using a ZYNQ SoC for the SDR platform. The ARM processor is used to generate and receive the low frequency baseband signals through the AXI-Lite interface, and the FPGA fabric on-chip will handle most of the heavy computations including DUC and DDC. The FPGA also makes it possible to connect multiple high-speed ADCs and DACs without adding additional peripheral and circuits. The high bandwidth between the ARM processor and FGPA allows for real-time communication and add expandability to the system. In our previously published papers [8, 9], the efficiency and reconfigurability of using ZYNQ SoC for high speed signal processing system design is presented.

IV. Experiments and Results

PZT transducer is used as the energy transformer to convert the electric energy to ultrasonic wave. The PZT transducer can generate and receive ultrasonic waves at its resonant frequency. Figure 4 shows a practical test setup for conducting ultrasonic

communication. With the support of a 3D printed holder, PZT transducers are mounted on the two sides of the acrylic column. Ultrasonic coupling gel with medium viscosity is used on the contact surface of the acrylic column and on the PZT transducers to ensure a better transmission and reception of the ultrasonic signals. With this test setup bulk waves are generated for ultrasonic communications under ideal conditions.

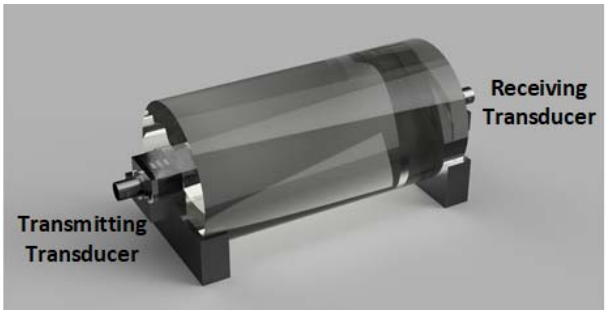

Figure 4. Test Setup A - Direct Transmitting and Receiving

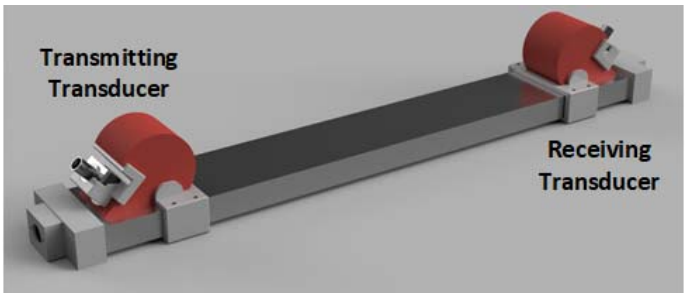

Figure 5. Test Setup B – Transmitting and Receiving with an Oblique Angle

In Figure 5, the ultrasonic signal is transmitted through a solid bar with oblique angle wedges. 3D printed sliding fixtures are used to move the transducers along the solid bar. Two 2.5 MHz piezoelectric transducers are used for transmitting and receiving ultrasonic signals. Both wedges are 60-degree. The distance between the two transducers is defined by the point where the main beam of ultrasonic signal is supposed to enter the metal bar to the point where the receiver transducer should pick it up.

Figure 6 shows the modulation and de-modulation of a 312 kbps baseband signal modulated using on-off keying (OOK) method. In this scenario, the quadrature component is set to 0 and in-phase component is either 0 or 1. Figure 6b shows the received signal. Figure 6c is the de-modulated IQ data obtained by using the DDC on the FPGA. The Test Setup A (see Figure 4) is utilized, and the channel is acrylic column (3-inch diameter and 3-inch length). Two 2.5 MHz PZT transducers are used as the transmitter and the receiver.

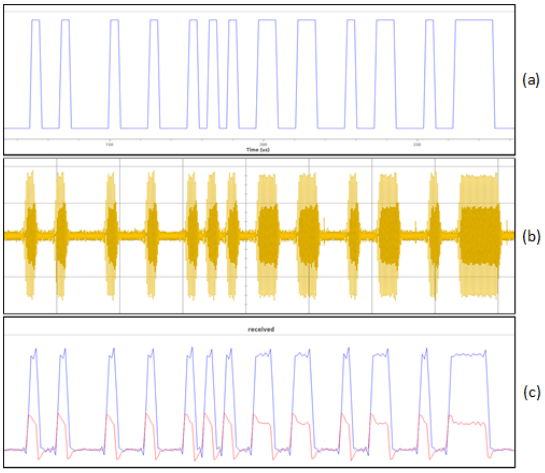

Figure 6. Simple OOK Transmitting and Receiving

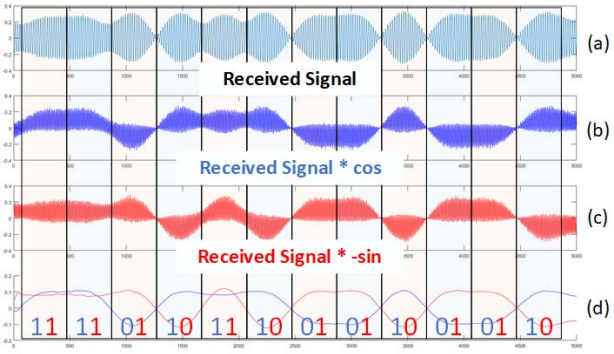

Figure 7. QPSK De-Modulation Procedures

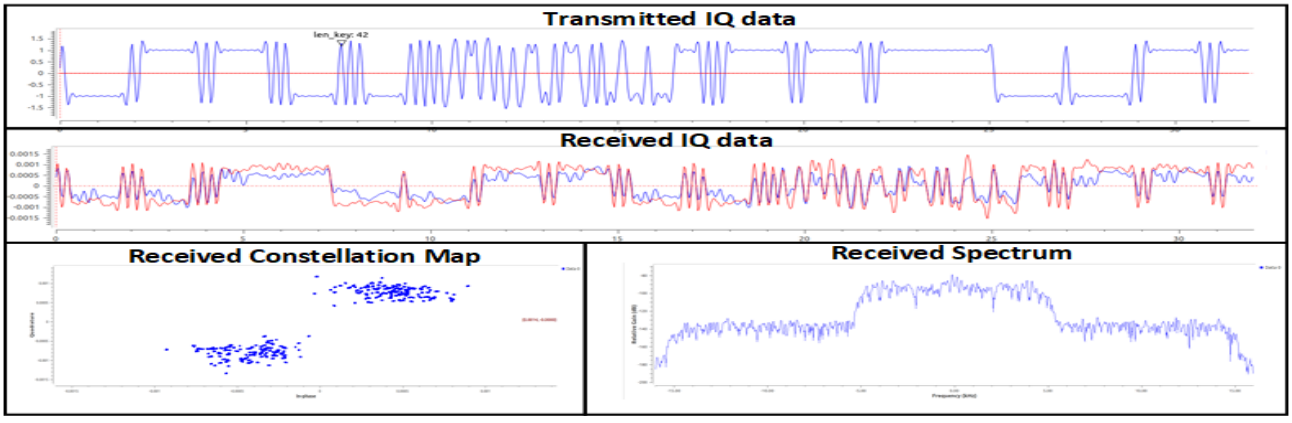

Figure 8. BPSK Transmitting and Receiving

With the same test setup (see Figure 4), Figure 7 shows the procedure to de-modulate a QPSK signal in MATLAB. The signal is generated by the transmitter which has the carrier frequency of 2.5 MHz. The symbol rate of the baseband signal is 125 k symbol per second which means that the signal is sent at the rate of 250 kbps. Figure 7a is a signal picked up by the receiver transducer and sampled by a MSOX2024A oscilloscope at the frequency of 50 MSPS. Figure 7b and Figure 7c are obtained by multiplying the signal with cosine and sinusoid signal with frequency of carrier frequency. This is to shift the target information from its carrier frequency back to its baseband. A low pass filter can extract the baseband signal perfectly as it shown in Figure 7d.

Figure 8 shows the transmitting and receiving signal using the binary phase shift keying (BPSK) when the Test Setup B (see Figure 5) is used. In this setup, the quadrature component is set to 0 and in-phase component is either -1 or 1. The distance between the two transducers is set to 0.5 meter. As expected, the BPSK modulation scheme offered the most robust performance for conducting communications using ultrasonic signals.

V. CONCLUSION

This paper presents the feasibility and advantages of using ultrasonic signal for communication in a diverse environment when other options for information transmission are not feasible. A Software Defined Radio (SDR) system that can be used for ultrasonic communications is introduced. This system is based on ZYNQ SoC (includes FPGA Fabric and ARM Processors) for information processing. Digital up converter and down converters on FPGA are used to process the high frequency signal in real-time. On-chip ARM processor will generate and receive the baseband signal. High speed ADC and DAC are used to transmit and receive RF ultrasonic signals. With this SDR platform, we can conduct a series of experiments with different modulation techniques, and various type of transducers and channel setups.

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